LCD MODULE

SPECIFICATION

Model:	UE047HD-HB31-L015A
Version:	V1.0
Date:	20200708

□ **Preliminary Specification** 样品规格书

□ **Final Specification** 量产规格书

Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

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REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	2020.07.08	Preliminary release	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB_Stripe
2) Interface Mode： MIPI
3) Driver IC：ST7703-G5-DP Touch IC：GT1151Q
4) Operation Temperature：-30~70℃
5) Storage Temperature：-40~80℃
6) Backlight Type：White LED
7) Display mode：Normally Black,
8) Pixel Density：315 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	
Screen Size	4.66	Inch	Diagonal
Resolution	720(W)*RGB*1280(H)	Dots	-
Interface	MIPI	-	4lanes
Module Power Consumption	0.6838	Watt	Typ.
Active Area	58.1(W)*103.3(H)	mm	-
Pixel pitch (W*H)	0.0269(W)*0.0807(H)	mm	-
CTP Module Size (W*H*D)	61(W)*111.15(H)*1.38(D)	mm	-
Luminance	450	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	16.7M	Colors	24bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	AVEE	-0.3	4.6	V	Note1
Power supply2 voltage	AVDD	-0.3	6.6	V	
Power supply3 voltage	IOVCC	-6.6	0.3	V	
LED forward current	I_F	-0.001	20	mA	For each led,Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	℃	Note1,2
Storage temperature	T_{st}	-30	80	℃	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH .

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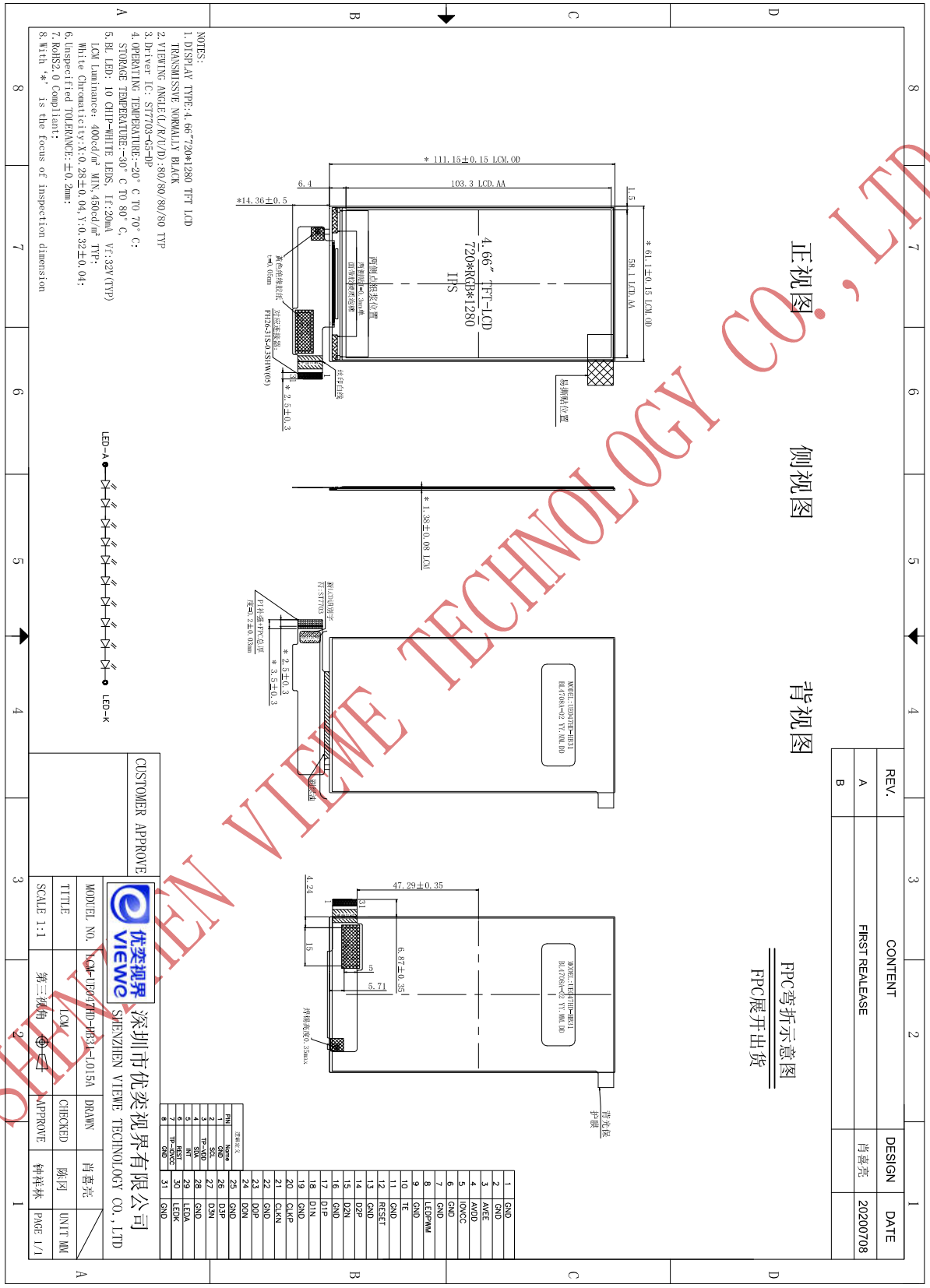
3. MECHANICAL DRAWING



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4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1-2	GND	P	Power Ground
3	AVEE	P	Negative input analog power for driver IC use
4	AVDD	P	Positive input analog power for driver IC use
5	IOVCC	P	Power supply for logic circuits and IO pads(1.8V)
6-7	GND	P	Power Ground
8	LEDPWM	O	LED PWM Oouput
9	GND	P	Power Ground
10	TE	O	Tearing effect outputsignal. If not used, please let this pin open
11	GND	P	Power Ground
12	RESET	I	The signal will reset the LCM, Signal is active low.
13	GND	P	Power Ground
14	D2P	I	MIPI-DSI data lane 2 positive-end input pin
15	D2N	I	MIPI-DSI data lane 2 negative-end input pin
16	GND	P	Power Ground
17	D1P	I	MIPI-DSI data lane 1 positive-end input pin
18	D1N	I	MIPI-DSI data lane 1 negative-end input pin
19	GND	P	Power Ground
20	CLKP	I	MIPI-DSI clock lane positive-end input pin
21	CLKN	I	MIPI-DSI clock lane negative-end input pin
22	GND	P	Power Ground
23	D0P	I/O	MIPI-DSI data lane 0 positive-end input pin
24	D0N	I/O	MIPI-DSI data lane 0 negative-end input pin
25	GND	P	Power Ground
26	D3P	I	MIPI-DSI data lane 3 positive-end input pin
27	D3N	I	MIPI-DSI data lane 3 negative-end input pin
28	GND	P	Power Ground
29	LEDA	P	Power supply for backlight anode
30	LEDK	P	Power supply for backlight cathode
31	GND	P	Power Ground

I：Input；O：Output；P：Power

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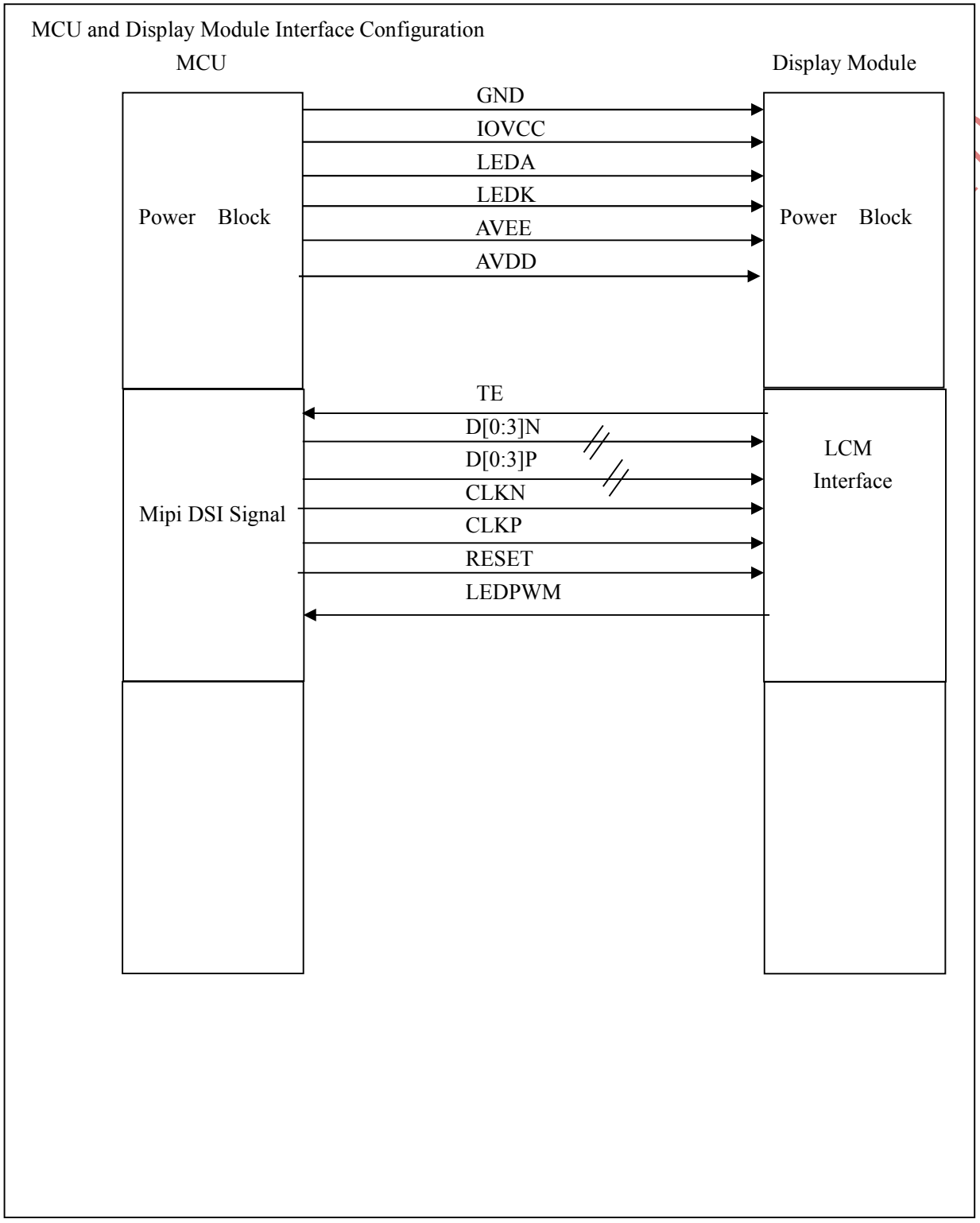
4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.65	1.8	2	V	-
Power Supply2 Voltage	AVEE	-6.2	-	-4.5	V	
Power Supply3 Voltage	AVDD	4.5	-	6.2	V	
Power Supply Current	I_{IOVCC}	-	27	-	mA	Note1
Power Supply Current	I_{AVEE}	-	1	-	mA	
Power Supply Current	I_{AVDD}		1		mA	
LCM Logic High level input voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
LCM Logic Low level input voltage	V_{IL}	VSSA	-	0.3IOVCC	V	-
LCM Logic High level output voltage	V_{OH}	0.8IOVCC	-	0.8IOVCC		I_{OH}=-1.0mA
LCM Logic Low level output voltage	V_{OL}	VSSA		0.2IOVCC		I_{OL}=+1.0mA
Panel Power Consumption	P_{LCM}	-	0.6838	-	Watt	Note1
Module Power Consumption	P_{ALL}	-	0.6252	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=2.8V,60Hz Refresh.

Note2: P_{ALL}= P_{LCM}+ P_{TP}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

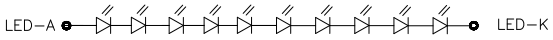
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	32	-	V	Note1
Forward Current	I_F	-	20	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.64	-	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			10		PCS	

(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module (6 LED Serial, 1 LED Parallel)。
For each LED ： I_F=20mA,V_F=3.2V(Typ.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



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5.3 Power On/Off Sequence

5.3.1 Power on timing

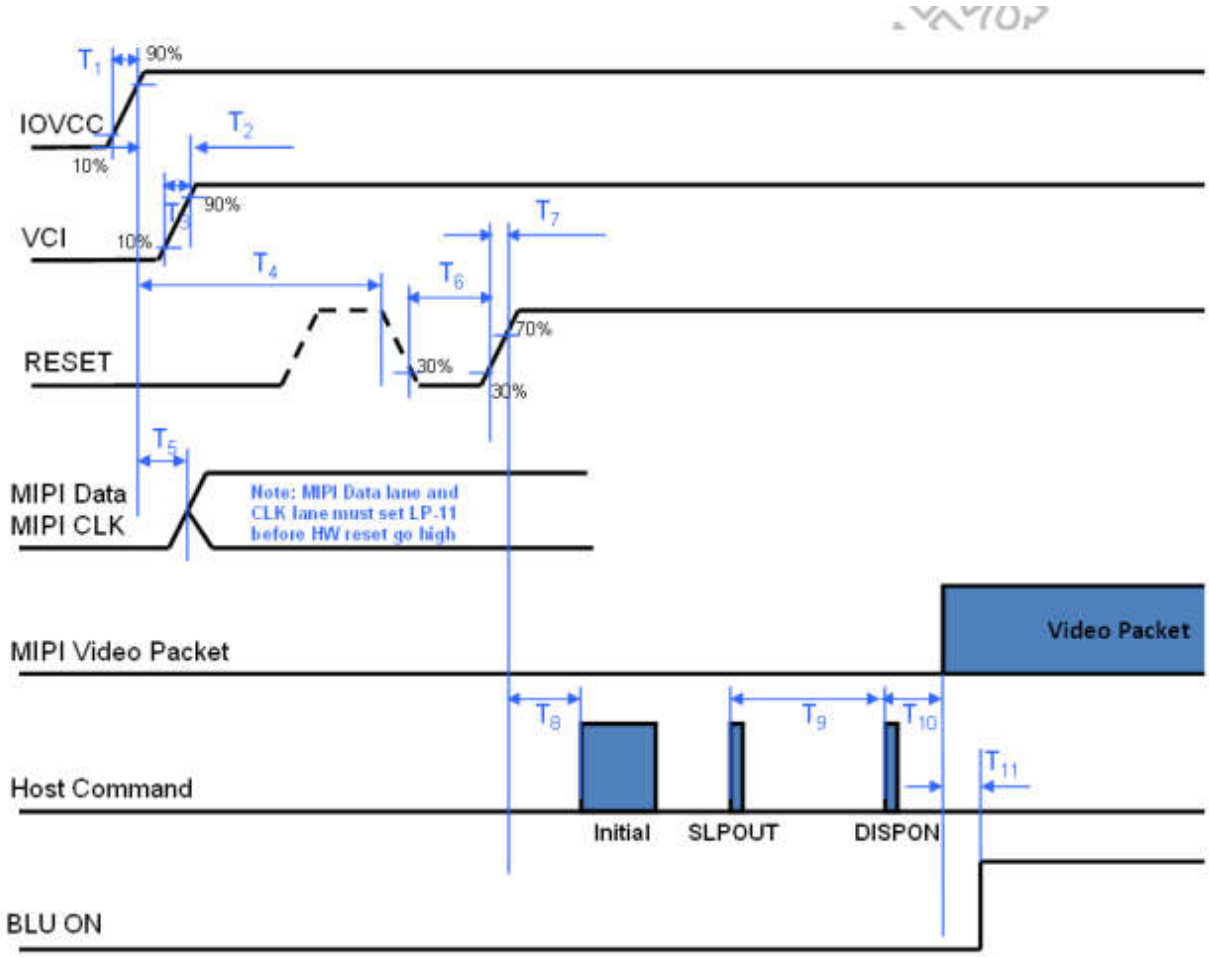

Figure 8-6: DSI Power On Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T1	0.01	-	10	ms
T2		No Limit		ms
T3	0.01	-	10	ms
T4	1	-	-	ms
T5	1	-	-	ms
T6	10	-	-	us
T7		No Limit		ns
T8	15	-	-	ms
T9	120	-	-	ms
T10		No Limit		ms
T11	100	150	-	ms

Table 8-1: DSI Power On Timing of Power IC Mode

5.3.2 Power off timing

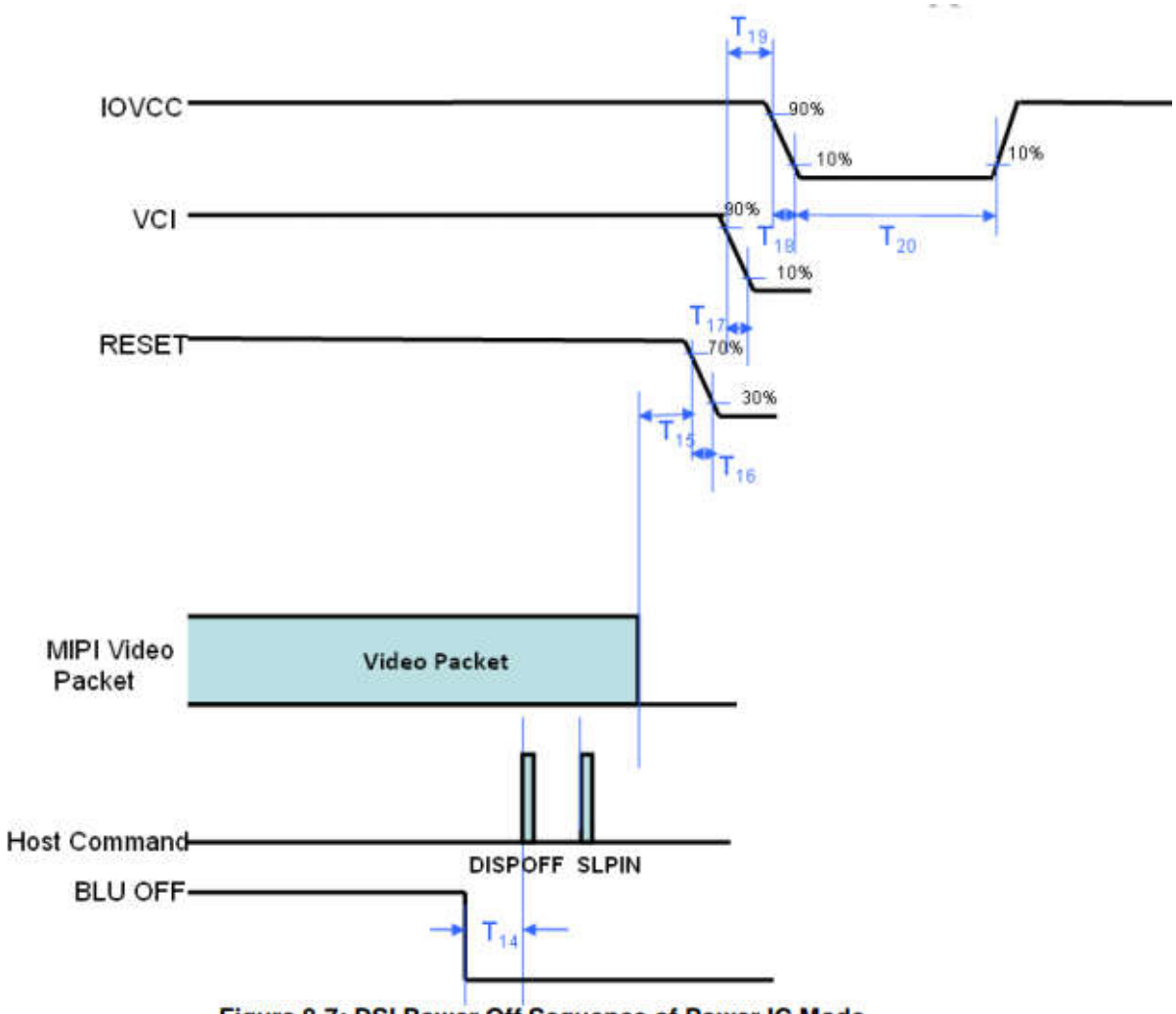

Figure 8-7: DSI Power Off Sequence of Power IC Mode

	Min.	Typ.	Max.	Unit
T14	40	100	-	ms
T15	10	-	-	ms
T16	No Limit			ms
T17	No Limit			ms
T18	No Limit			ms
T19	No Limit			ms
T20	100			ms

Table 8-2: DSI Power Off Timing of Power IC Mode

5.4 Timing Characteristics

5.4.1 DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps

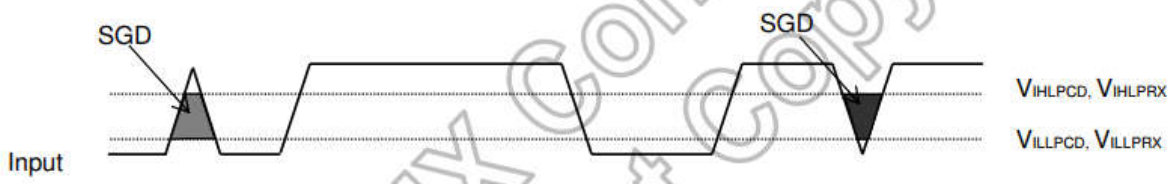

Figure 7.1: Input glitch rejections of low-power receivers

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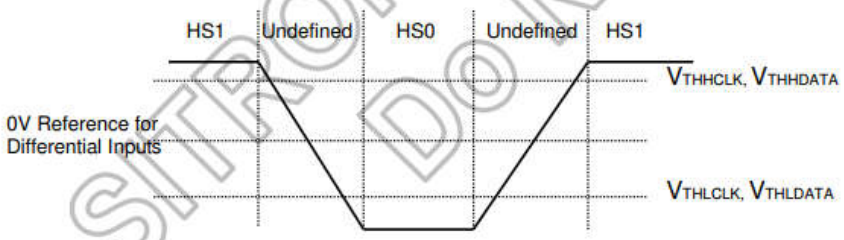
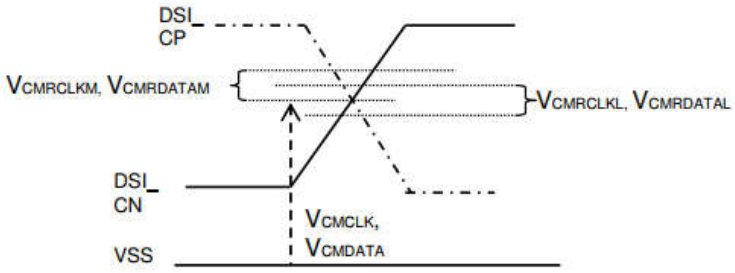
High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF





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5.4.2 AC Characteristics

High Speed Mode

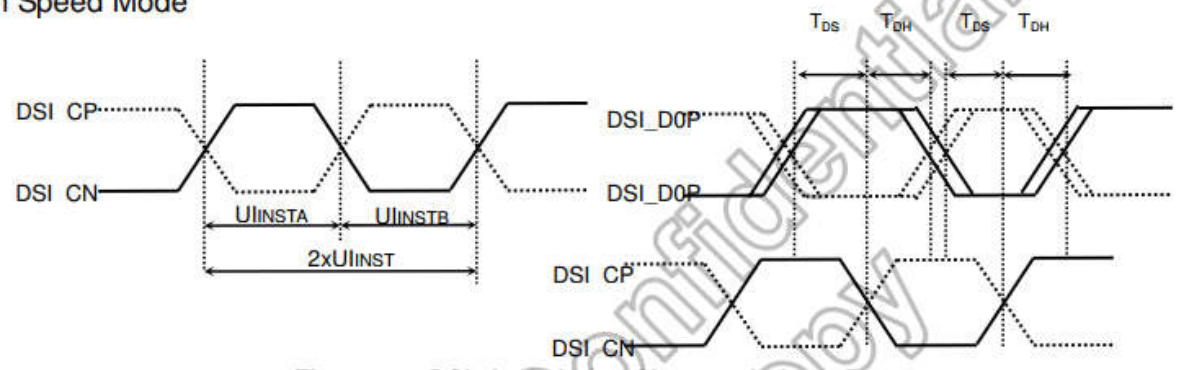

Figure 7.4: DSI clock timing Characteristics

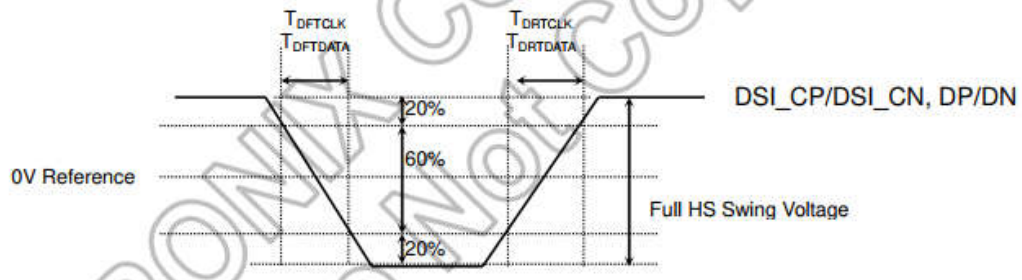

Figure 7.5: Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	TBD	-	25	ns
	UI instantaneous	UINSTA UINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

Table 7.3: DSI High Speed Mode Characteristics

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Low Power Mode

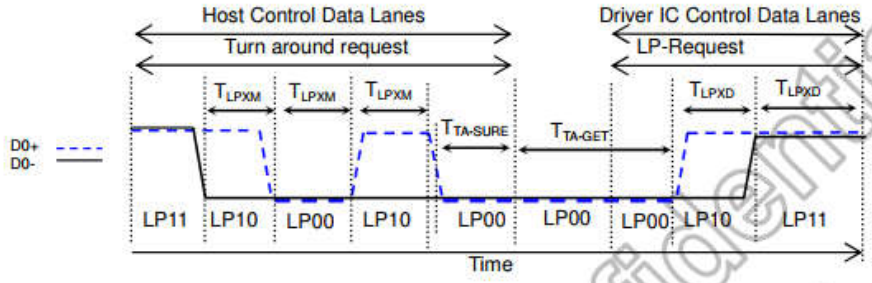

Figure 7.6: BTA from HOST to Display Module Timing

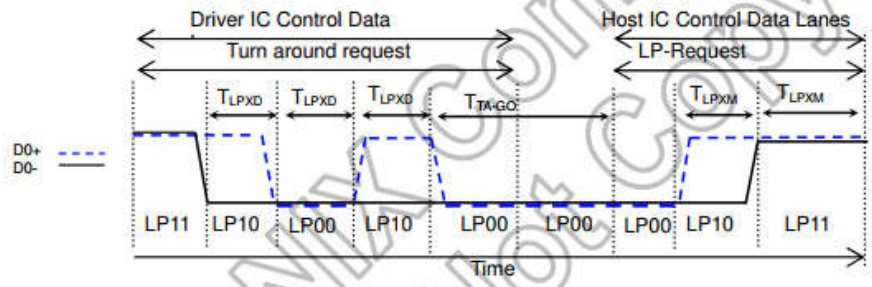

Figure 7.7: BTA from Display Module Timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	2xT_{LPXD}	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

Table 7.4: DSI Low Power Mode Characteristics

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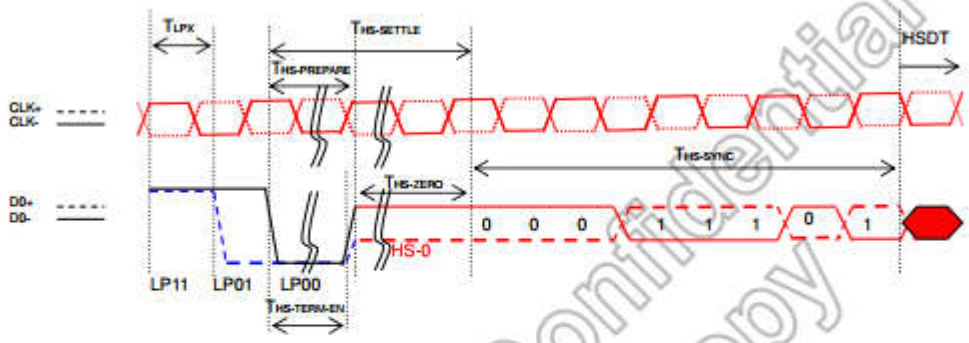
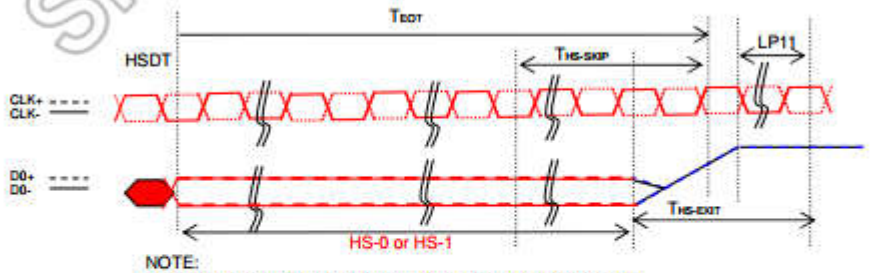
DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7.6: DSI Low Power Mode to High Speed Mode Timing

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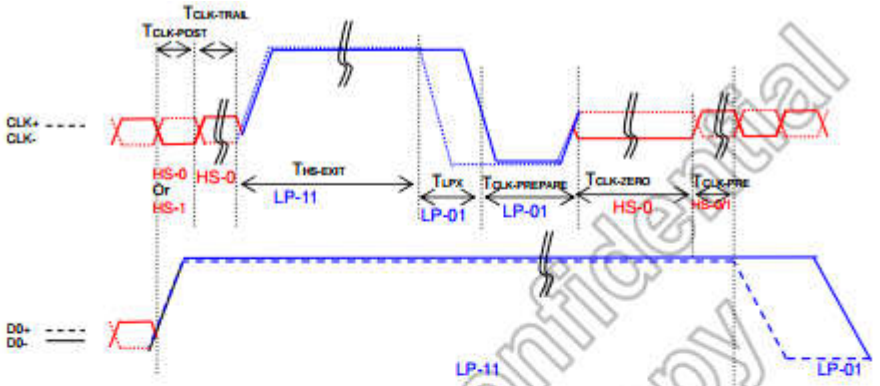

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7.7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

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5.5 Timing Diagram

Reset input timing

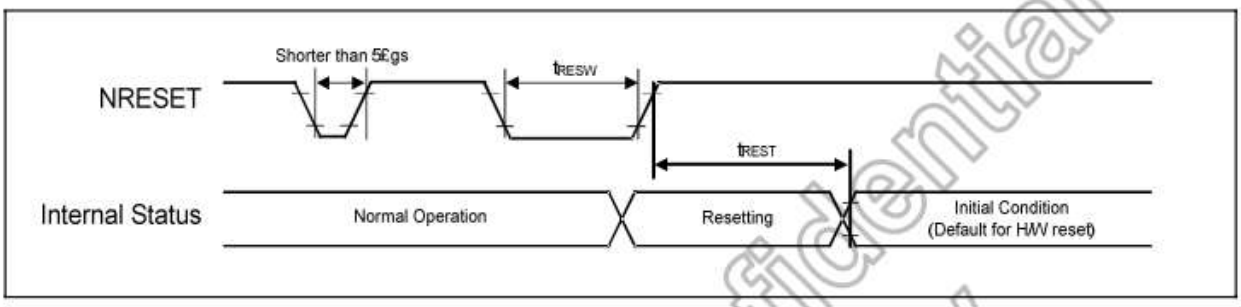


Figure 7.8: Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

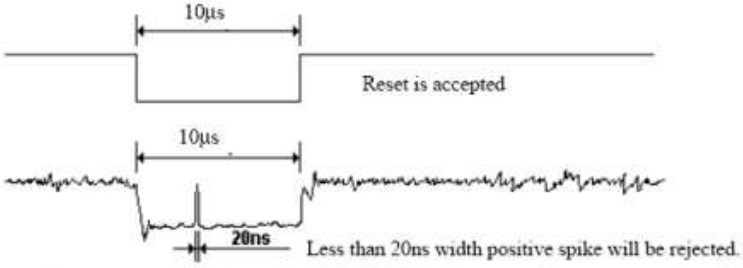
Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

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5.5.1 Horizontal Timings

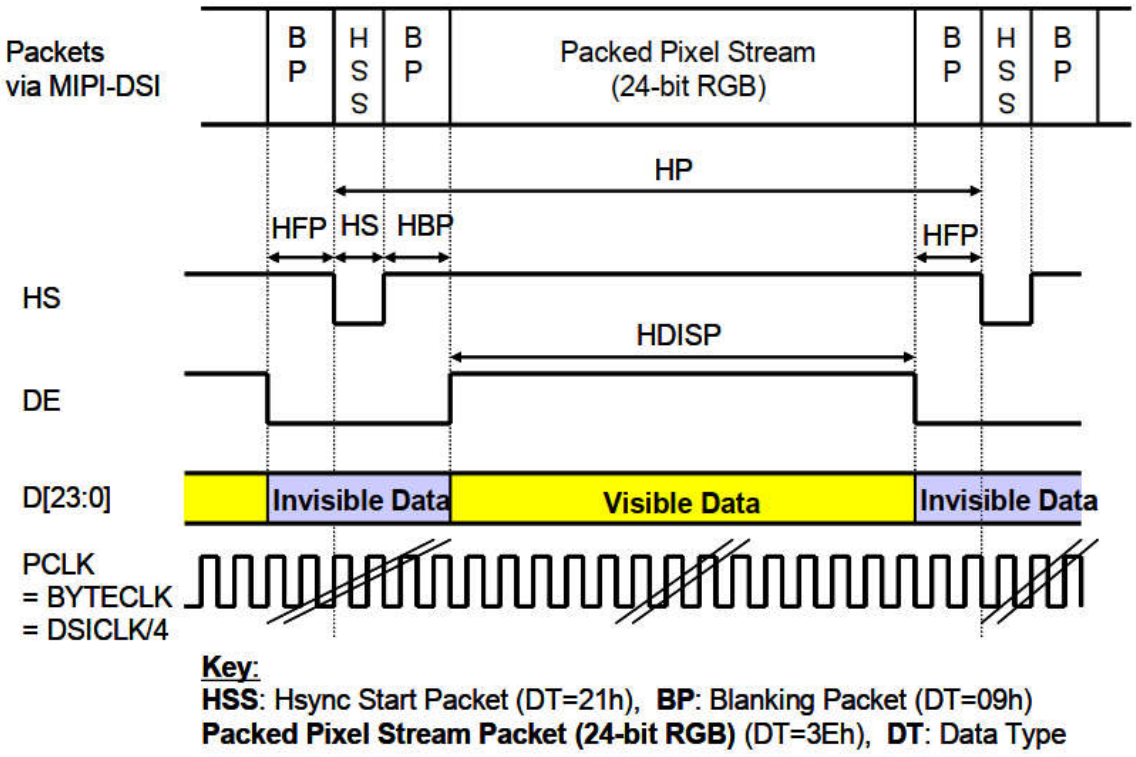

Figure 5 Horizontal Display Timing (MIPI-DSI)

Table 14 Horizontal Timing

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Horizontal front porch	HFP		PCLK	16	-	-	(2)
Horizontal data start point	-	HS+HBP	PCLK	16	-	-	(2)
Horizontal active area	HDISP		PCLK	480	640	640	(1), (2)

Notes: (1) Typical values are for 2xVGA (640 x 960) application.
(2) PCLK is pixel clock and same as BYTECLK that is generated by dividing DSICLK by 4.

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5.5.2 Vertical Timings

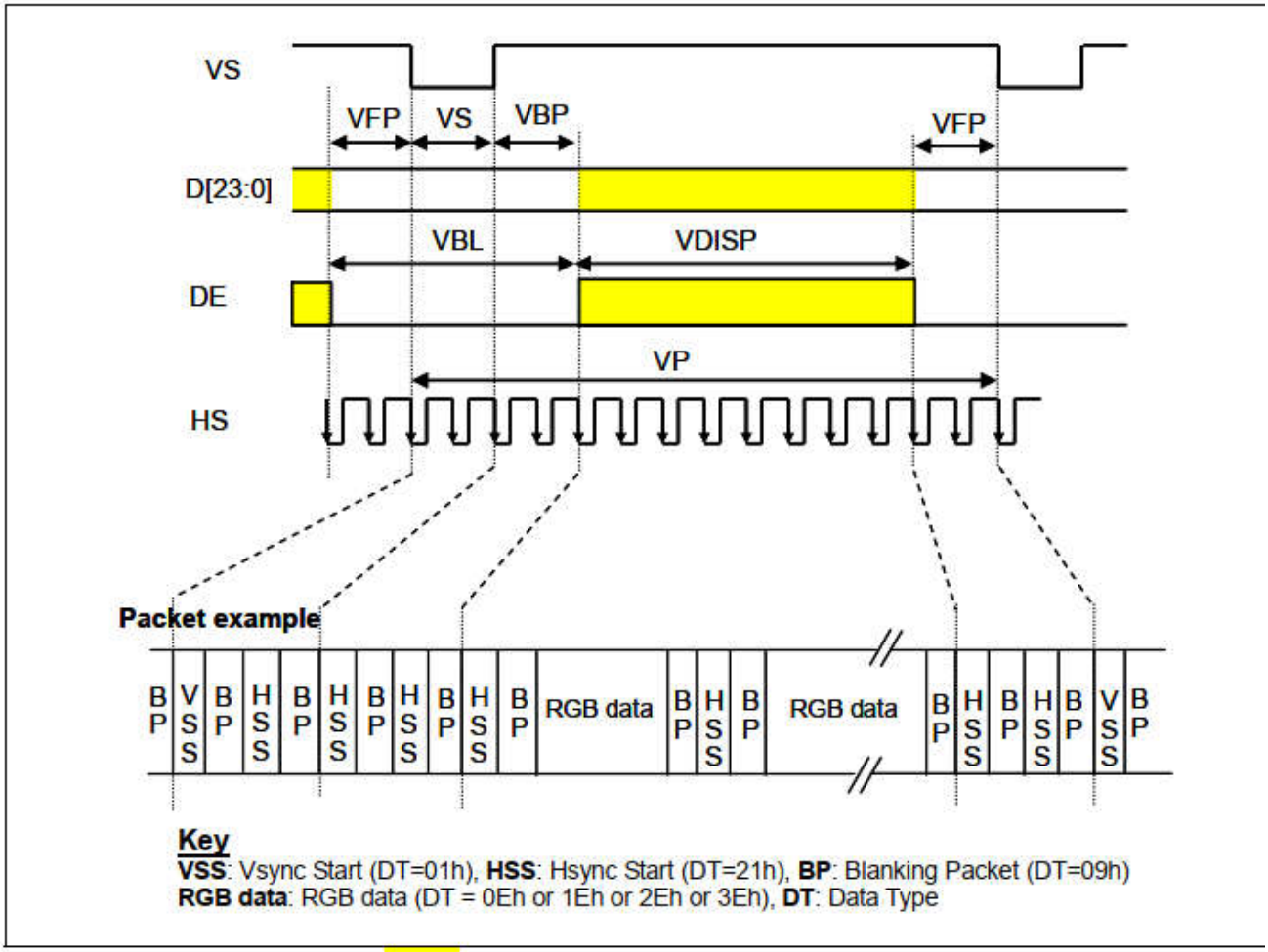

Figure 4 Vertical Display Timing (MIPI-DSI)

Table 13 Vertical Timing

Item	Symbol	Condition	Unit	Min.	Typ.	Max.	Notes
Vertical cycle	VP		line	-	1000		(1)
Vertical low pulse width	VS		line	-	16	-	(1), (2)
Vertical front porch	VFP		line	-	12		(1)
Vertical back porch	VBP		line	-	12		(1), (2)
Vertical data start point	-	VS+VBP	line	-	28	-	(1)
Vertical blanking period	VBL	VS+VBP+VFP	line	-	40	-	(1)
Vertical active area	VDISP		line	-	960	1080	(1)
(Vertical Refresh area)	(VRR)		Hz	-	60	-	(1)

Notes :(1) Typical values are for 2xVGA (640 x 960) application.
(2) VS +VBP is set as back porch by BP[3:0] bits @ C1h command.

5.5.3 Timing Parameters

Parameter	Symbol	Value			Unit
		Min.	Typ.	MAX.	
Bit rate per lane	BR_{PHY}	80	-	1000	Mbps
Active pixel per line	HACT	-	720	-	Pixels
Horizontal back porch	t_{HBP}	-	20	-	DCLK
Horizontal sync active	t_{HSA}	-	10	-	DCLK
Horizontal front porch	t_{HFP}	-	30	-	DCLK
Active pixel per frame	VACT	-	1280	-	H
Vertical back porch	t_{VBP}	-	24	-	H
Vertical sync active	t_{VSA}	-	4	-	H
Vertical front porch	t_{VFP}	-	16	-	H

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6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	1200	1500	-	-	Note(4)
NTSC Ratio	S	θ =0°	65	70	-	%	Note(7)
Luminance	L	θ =0°	-	450	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	-	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	25	30	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.03	0.28	+0.03	NTSC (x,y)	Note(6)
	W_Y			0.32			
	R_X			0.66			
	R_Y			0.31			
	G_X			0.25			
	G_y			0.57			
	B_X			0.13			
	B_Y			0.09			
Viewing Angle	Θ_1	C/R>10	-	80	-	Degree	Note(1)
	θ_R		-	80	-		
	θ_U		-	80	-		
	θ_D		-	80	-		

Test Conditions:

1. The ambient temperature is+25℃.
2. The test systems refer to Note 8.

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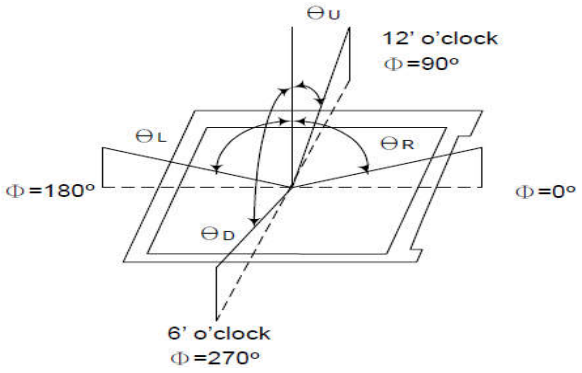
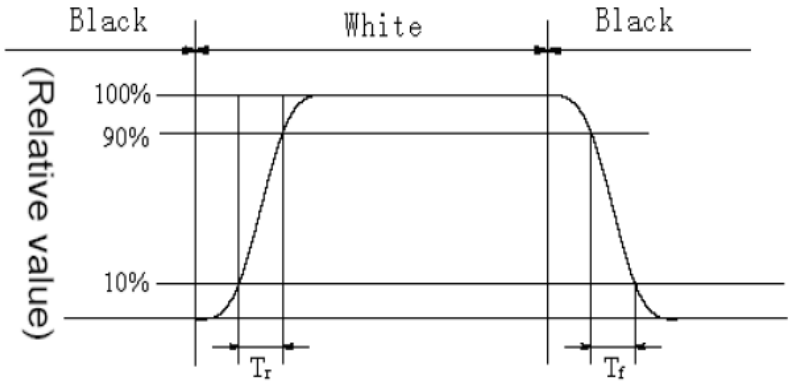
Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

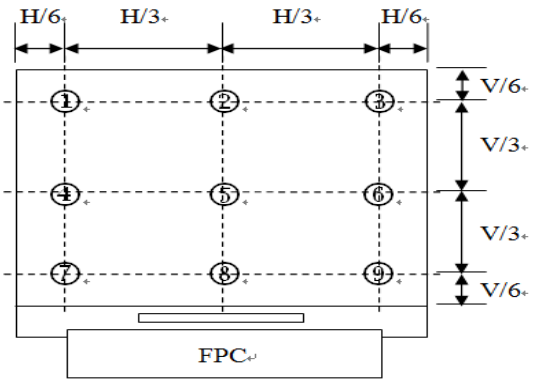


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

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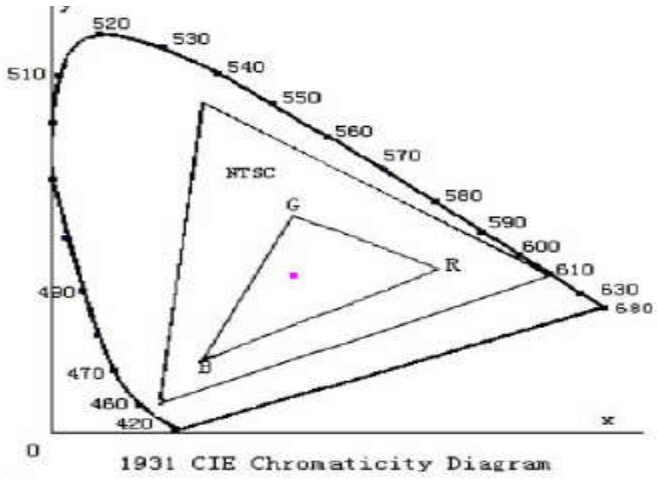
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

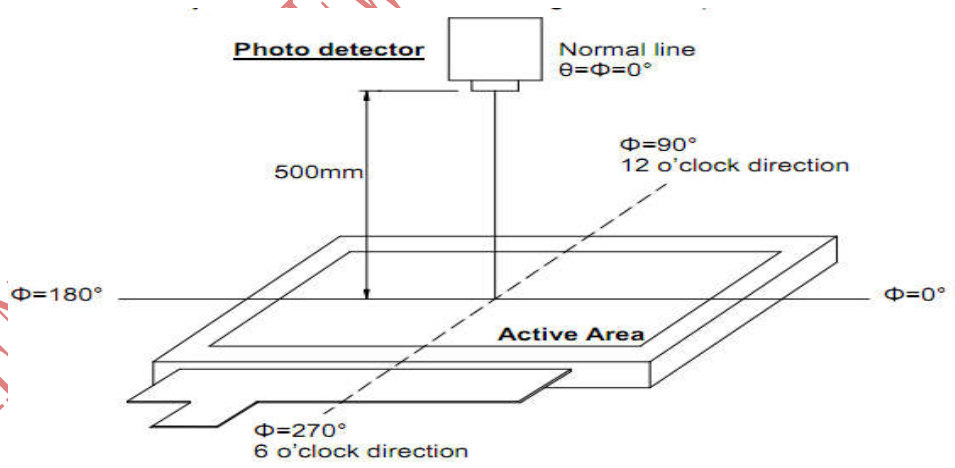
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-40°C/30min Δ+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	70°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

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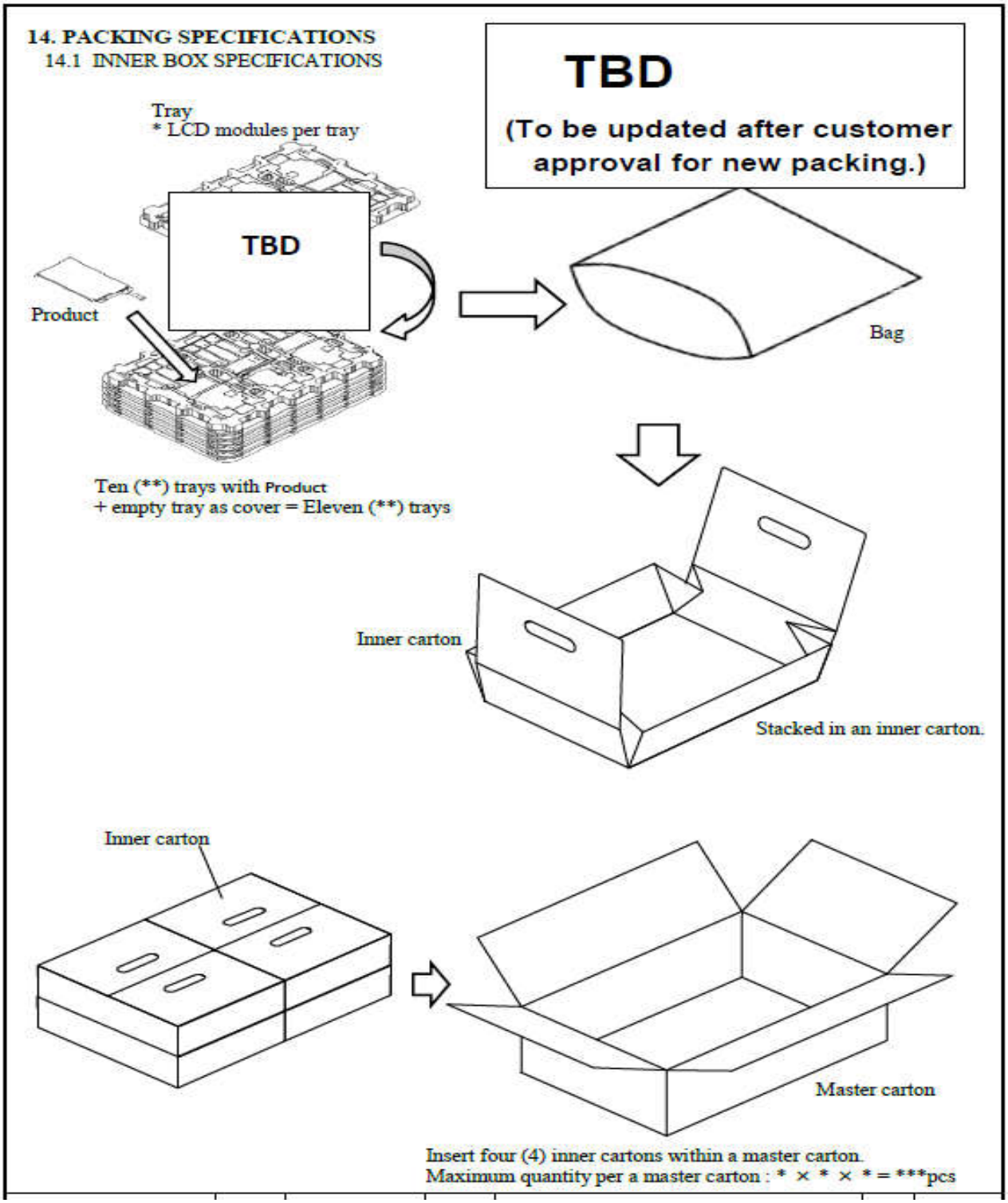
8. PACKAGE DRAWING