LCD MODULE

SPECIFICATION

Model:	UE034WX-AB39-L001A
Version:	V1.0
Date:	20220514

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Customer Confirmation 客户确认

Approved by	Notes

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REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20220514	Preliminary release	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB_Stripe
2) Interface Mode： MIPI 3lane
3) Driver IC：JD9365DA-H3
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode：Normally Black
8) Pixel Density：232 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	
Screen Size	3.4	Inch	Diagonal
Resolution	800(W)*3(RGB)*800(H)	Dots	-
Interface	MIPI	-	3lanes
Module Power Consumption	TBD	Watt	Typ.
Active Area	87.60（⌀ ）	mm	Typ.
Pixel pitch (W*H)	0.0365(W)*0.1095(H)	mm	Typ.
Module Size (W*H*D)	94.90(W)*96.95(H)*2.22(D)	mm	Typ.
Luminance	650	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	16.7M	Colors	24bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply2 voltage	IOVCC	-0.3	3.6	V	
LED Reverse Voltage	V_R	-	6.6	V	For each led,Note1
Operating temperature	T_{op}	-20	70	°C	Note1,2
Storage temperature	T_{st}	-30	80	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.

Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

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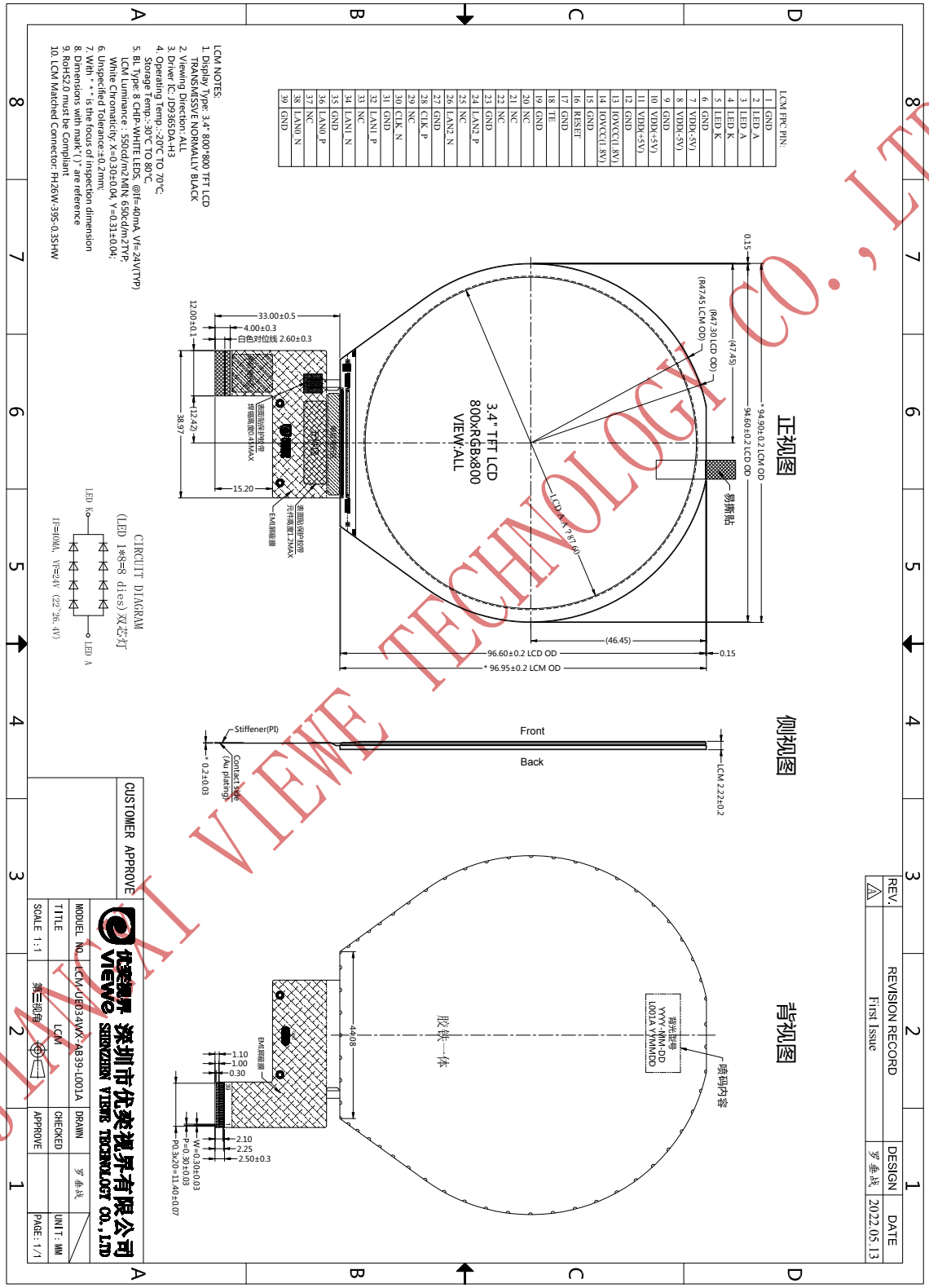
3. MECHANICAL DRAWING



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4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	GND	P	Power Ground
2-3	LEDA	P	LED Anode
4-5	LEDK	P	LED Cathode
6	GND	P	Power Ground
7-8	VDD(-5V)	P	-5V INPUT
9	GND	P	Power Ground
10-11	VDD(+5V)	P	+5V INPUT
12	GND	P	Power Ground
13-14	IOVCC(1.8V)	P	Power supply 1.8V
15	GND	P	GND
16	RESET	I	Global Reset Pin
17	GND	P	Power Ground
18	TE	I	Tearing effect output
19	GND	P	Power Ground
20-22	NC	-	No connect
23	GND	P	Power Ground
24	LAN2_P	I	MIPI lane 2+
25	NC	-	No connect
26	LAN2_N	I	MIPI lane 2-
27	GND	P	Power Ground
28	CLK_P	I	MIPI clock+
29	NC	-	No connect
30	CLK_N	I	MIPI clock-
31	GND	P	Power Ground
32	LAN1_P	I	MIPI lane 1+
33	NC	-	No connect
34	LAN1_N	I	MIPI lane 1-
35	GND	P	Power Ground
36	LAN0_P	I	MIPI lane 0+
37	NC	-	No connect
38	LAN0_N	I	MIPI lane 0-
39	GND	P	Power Ground

I：Input；O：Output；P：Power

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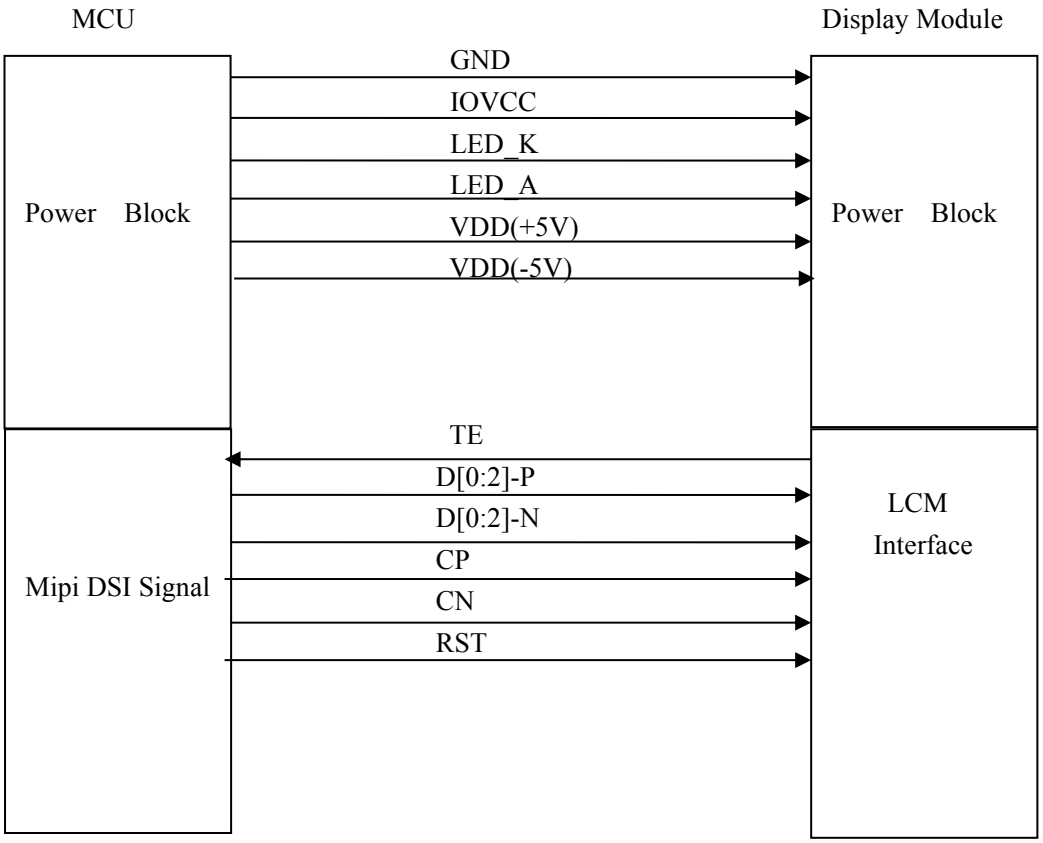
4.2 Block Diagram

MCU and Display Module Interface Configuration



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5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.71	1.8	1.89	V	-
Power Supply Current	I_{IOVCC}	-	TBD	-	mA	
Logic Input High Voltage	V_{IH}	0.7* IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3* IOVCC	V	-
Panel Power Consumption	P_{IOVCC}	-	TBD	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	TBD	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,IOVCC=1.8V,60Hz Refresh.

Note2: P_{LCM}= P_{IOVCC}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	22	24	26.4	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}		0.96	-	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			8		PCS	

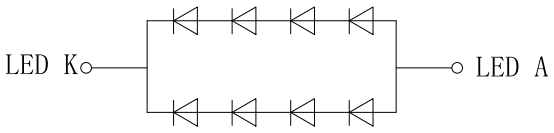
(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module (4 LED Serial, 2 LED Parallel)。
For each LED ： I_F=20mA,V_F=6.0V(Typ.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.

CIRCUIT DIAGRAM

(LED 1*8=8 dies)双芯灯



IF=40MA, VF=24V (22~26.4V)

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5.3 Power On/Off Sequence

To prevent the device damage from latch up and Improve subjective display effect,the power ON/OFF sequence shown below must be followed.

During power off, if the display module is in the SLPOUT mode, VCI, VCIP and VCCD/IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI, VCIP and VCCD/IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display panel between end of Power On Sequence and before receiving SLPOUT command. Also between receiving SLPOUT command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 9.5.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

There is not a limit for Rise/Fall time on VCI, VCIP and VCCD/IOVCC.

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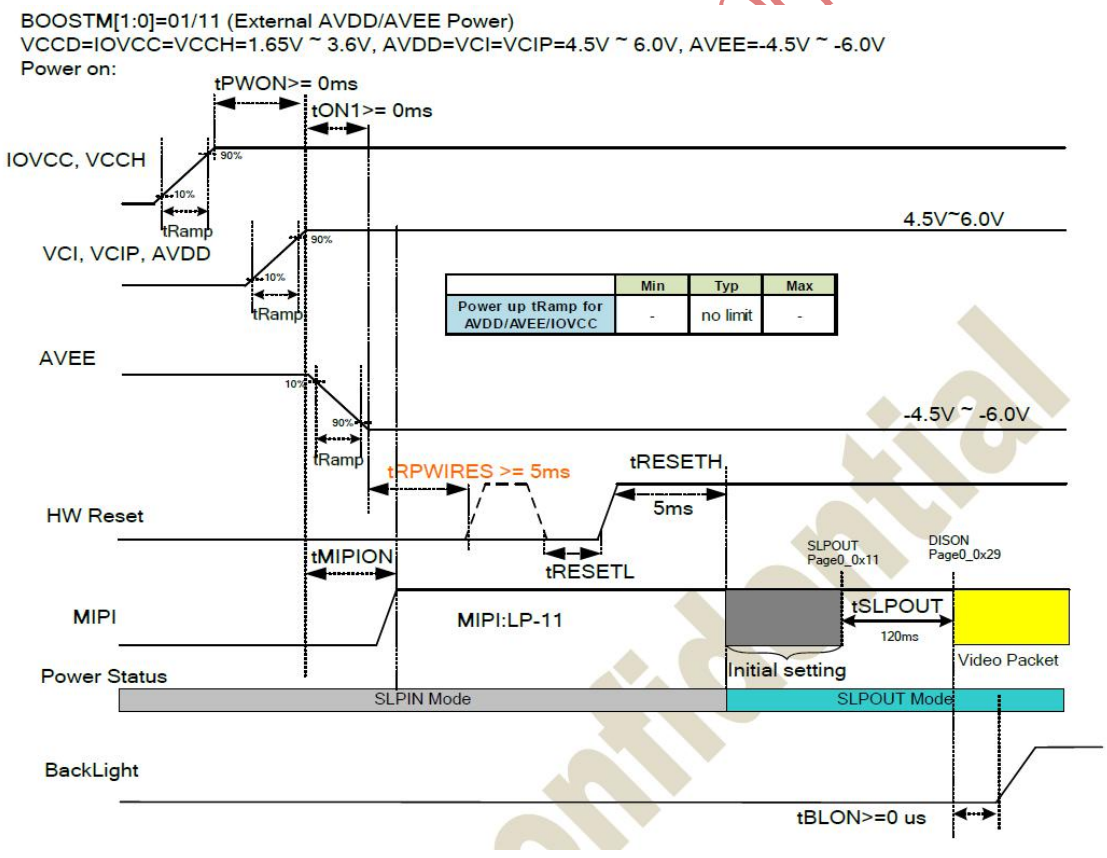
5.3.1 Power On Sequence

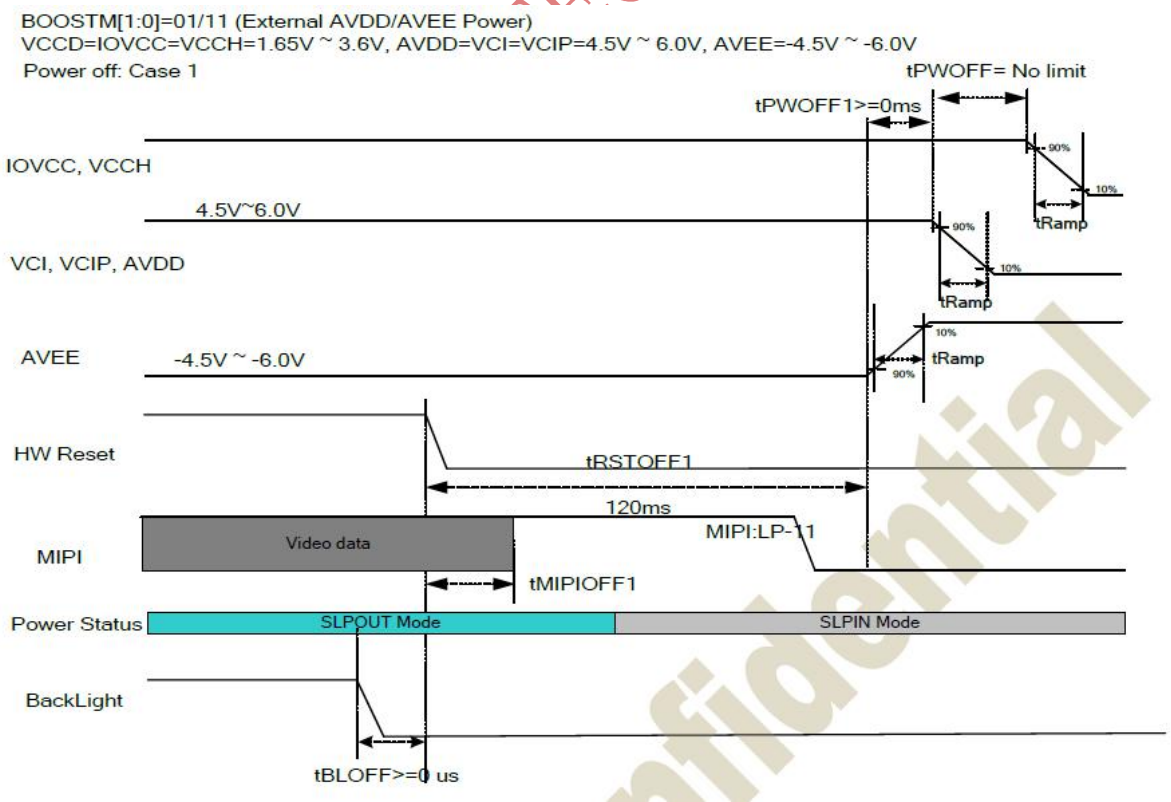
Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWON	0	-	-	ms	
tON1	0	-	-	ms	
tMIPI-ON	0	-	tRPWIRES	ms	
tRPWIRES	5	-	-	ms	
tRESETL	10	-	-	us	
tRESETH	5	-	-	ms	
tSLPOUT	120	-	-	ms	
tBLON	0	-	-	ms	



5.3.2 Power Off Sequence

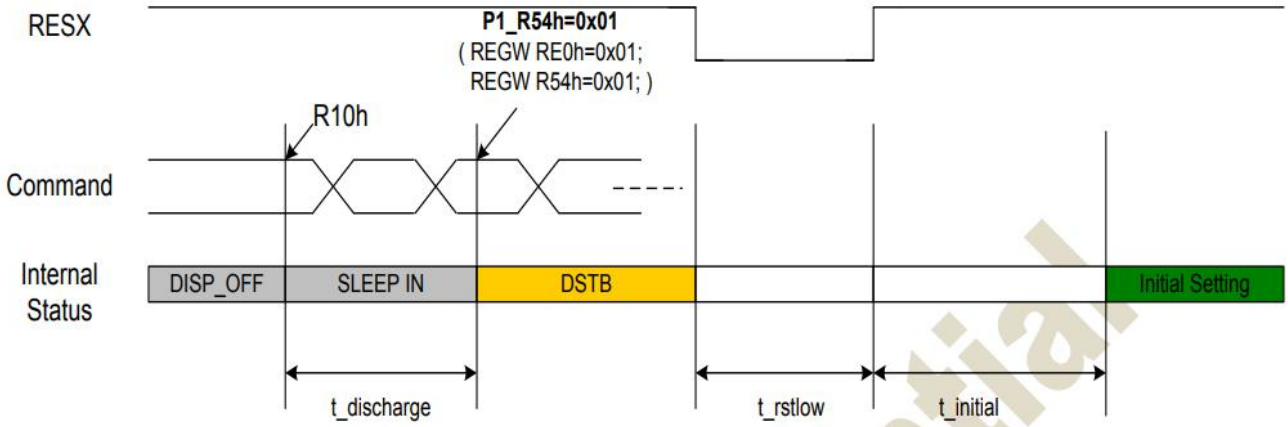
For the power off case2, DISOFF command and tDISOFF are optional. That means t_{CMD_OFF} could be followed by the SLPIN command and tSLPIN , without DISOFF command and tDISOFF.

Symbol	Min	Typ	Max	Unit	Remark
tRamp	-	no limit	-	us	
tPWOFF	0	-	-	ms	
tPWOFF1	0	-	-	ms	
tPWOFF2	0	-	-	ms	
tMIPIOFF1	0	-	-	ms	power off case 1
tRSTOFF1	120	-	-	ms	power off case 1
tMIPIOFF2	0	-	-	ms	power off case 2
tRSTOFF2	0	-	-	ms	power off case 2
tCMD_OFF	1	-	-	ms	power off case 2
tDISOFF	50	-	-	ms	power off case 2
tSLPIN	100	-	-	ms	power off case 2
tBLOFF	0	-	-	ms	



5.3.3 Deep standby Flow

The figure below illustrates deep standby flow, :



Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{discharge}$	Sleep in into DSTB delay time	100	-	-	ms	
	t_{rstlow}	Reset low pulse	5	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	10	-	-	ms	

Note 1) $t_{_discharge}$ suggested delay time over 100ms.

Note 2) $t_{_initial}$ suggested delay time over 10ms..

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5.4 Timing Characteristics

5.4.1 Reset input timings

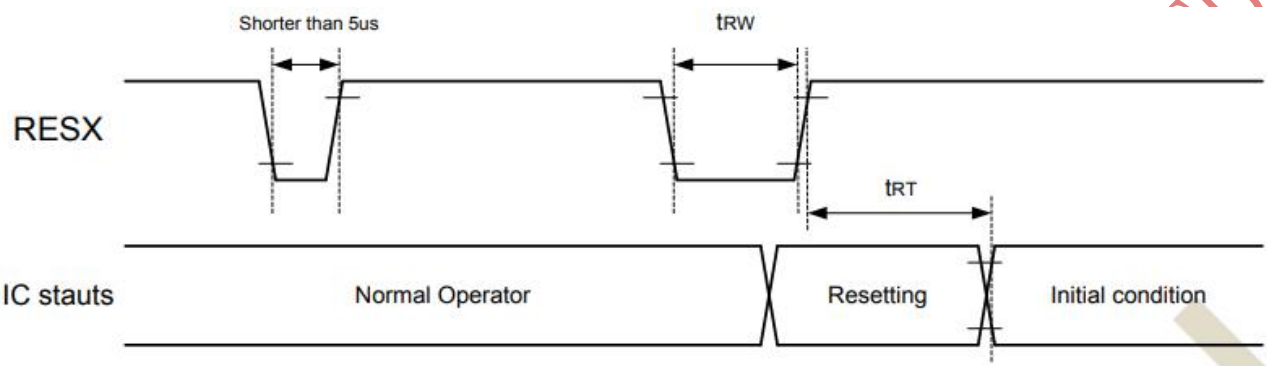

Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	μs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

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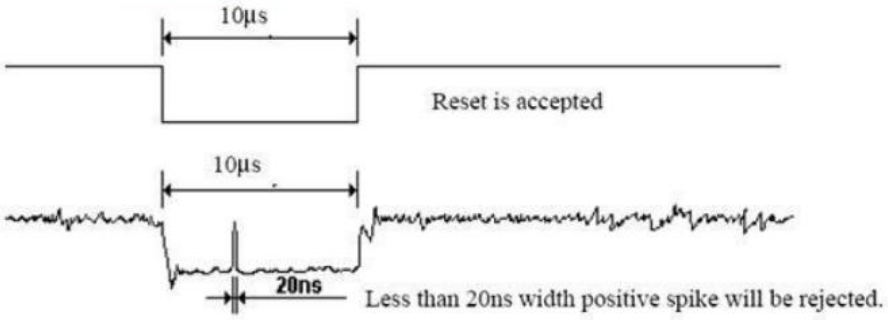
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

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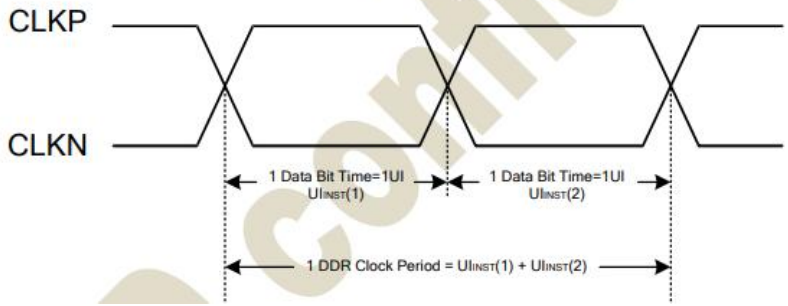
5.4.2 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.



The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

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The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 850bps of 1 data lane 24-bit data format/ 630Mbps of 1 data lane 18-bit data format/ 560Mbps of 1 data lane 16-bit data format.
(4) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(6) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

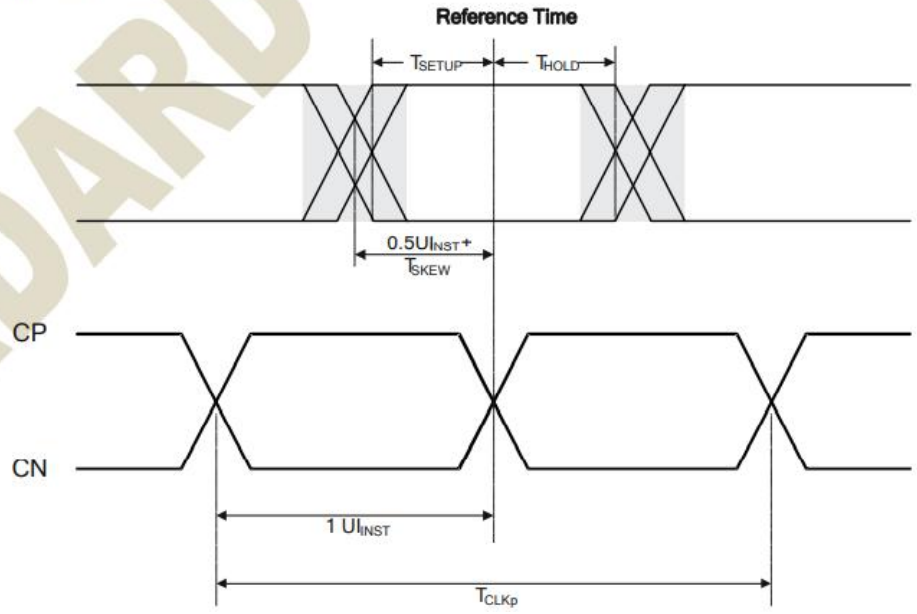
Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.



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Data-Clock Timing Specifications

The Data-Clock timing specifications are shown in Table 13.12. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 13.12 are specified as a part of this value.. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

Table 11.12: Data to Clock Timing Specifications

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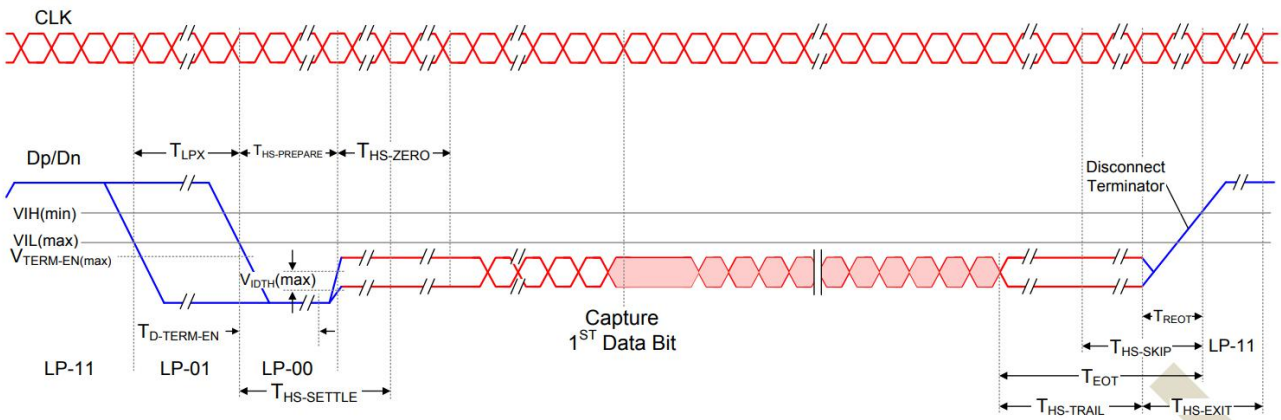
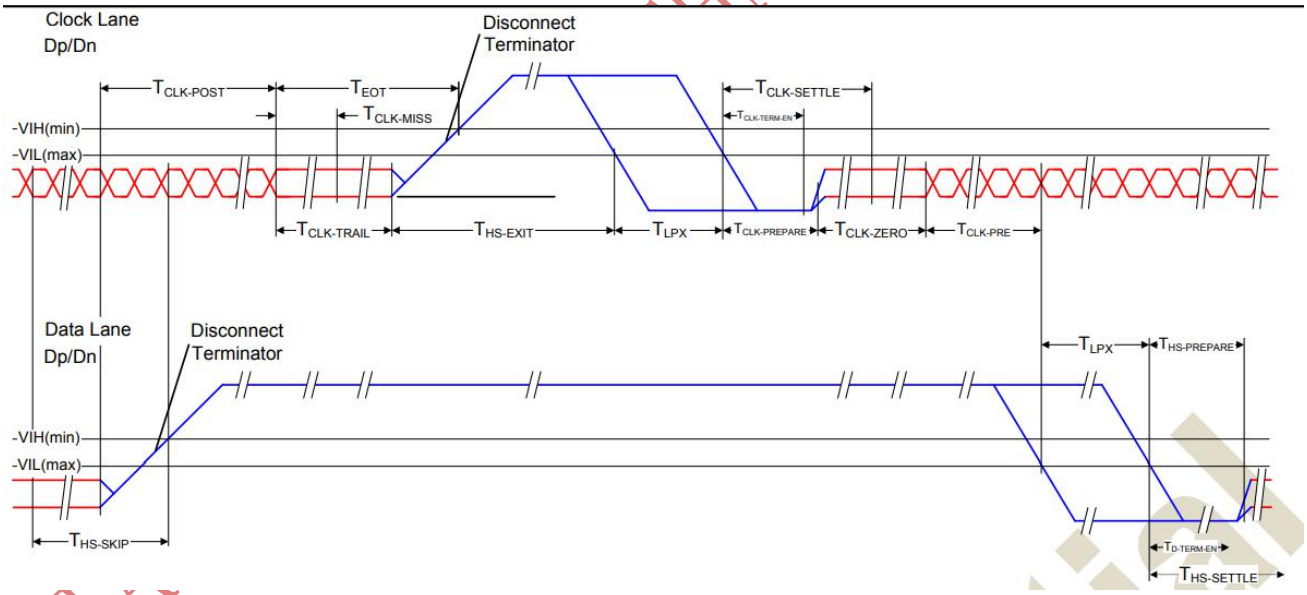
5.4.3 Burst Mode Data Transmission



Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns



Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

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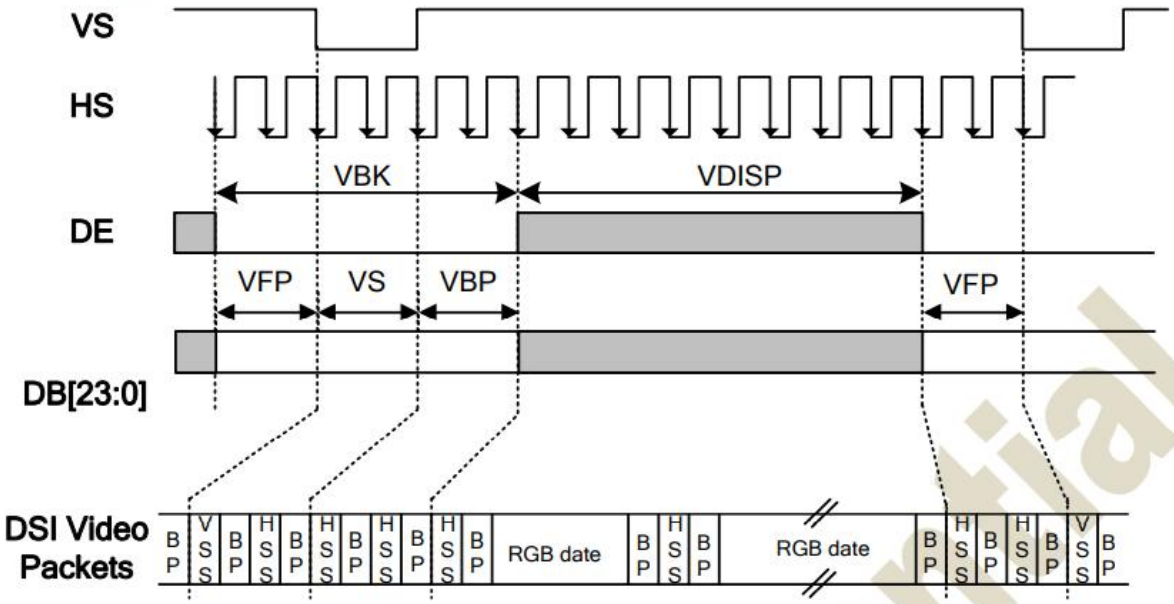
5.4.4 Timings for DSI Video mode

Vertical Timings



Horizontal Timings

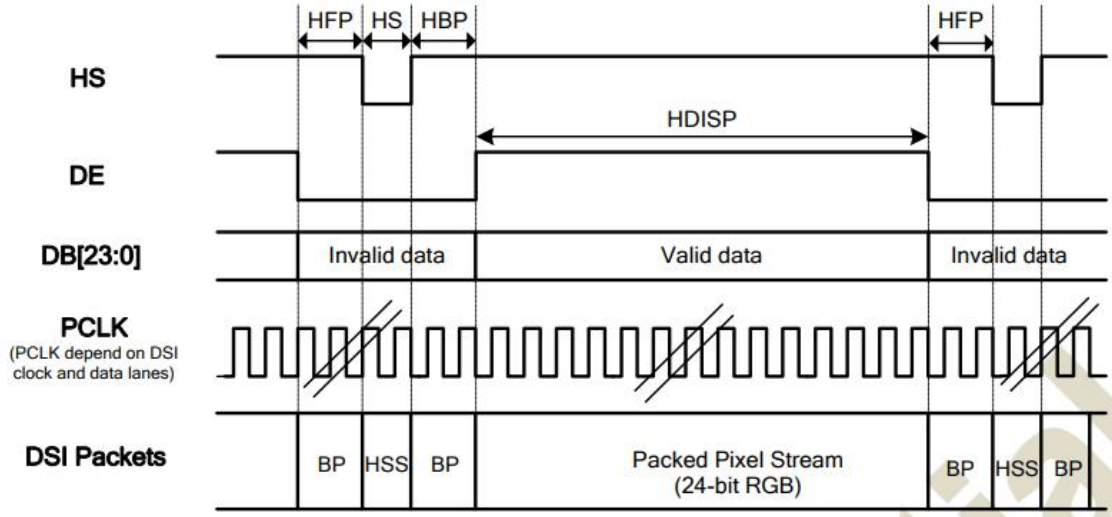


Figure 11.10: Horizontal Timing for DSI Video mode I/F

6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	1000	1200	-	-	Note(4)
NTSC Ratio	S	θ =0°	65	70	-	%	Note(7)
Luminance	L	θ =0°	-	650	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	70	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	30	35	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	TBD	+0.04	NTSC (x,y)	Note(6)
	W_Y			TBD			
	R_X			0.667			
	R_Y			0.323			
	G_X			0.271			
	G_y			0.591			
	B_X			0.134			
	B_Y			0.121			
Viewing Angle	Θ_l	C/R>10	80	85	-	Degree	Note(1)
	θ_R		80	85	-		
	θ_U		80	85	-		
	θ_D		80	85	-		

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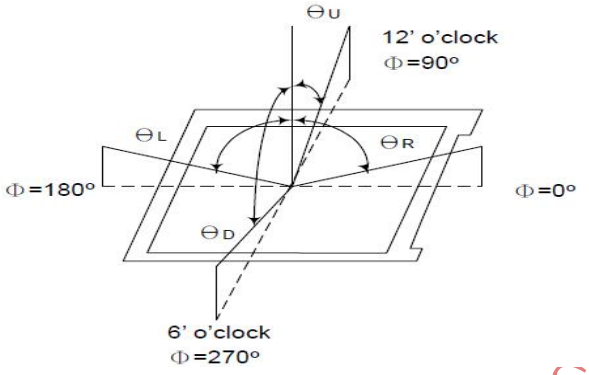
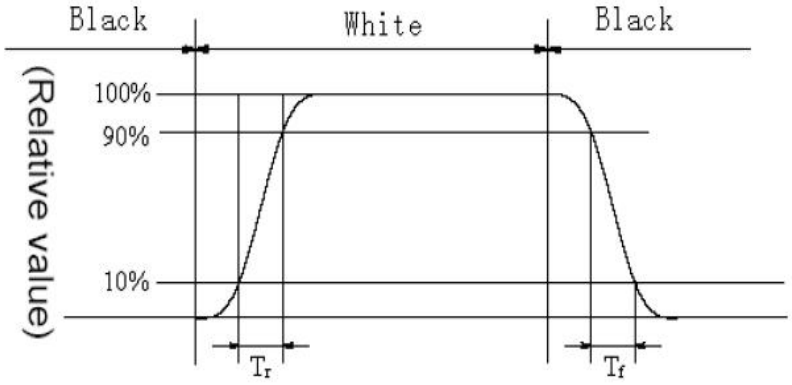
Test Conditions:

1. the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

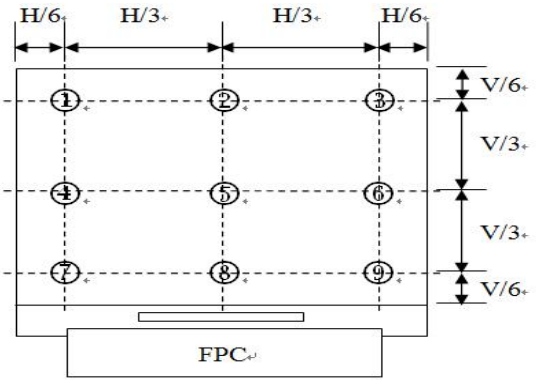


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

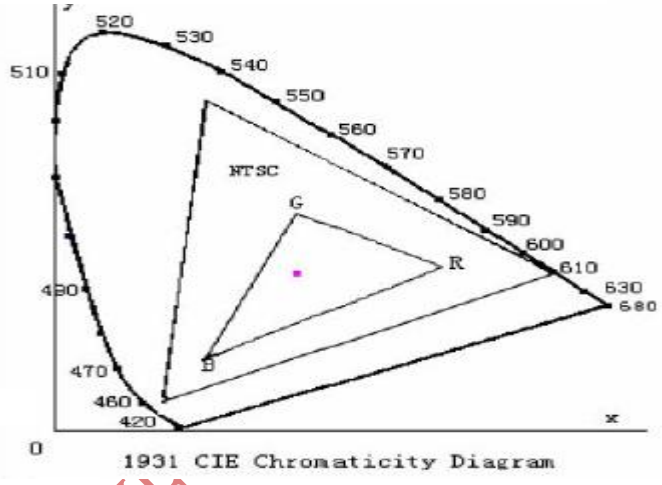
Note 5 Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

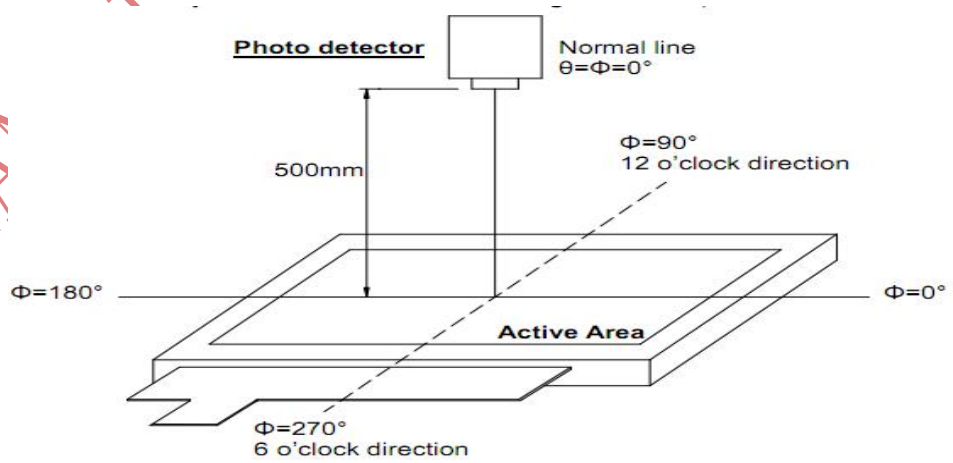
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min Δ+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	70°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

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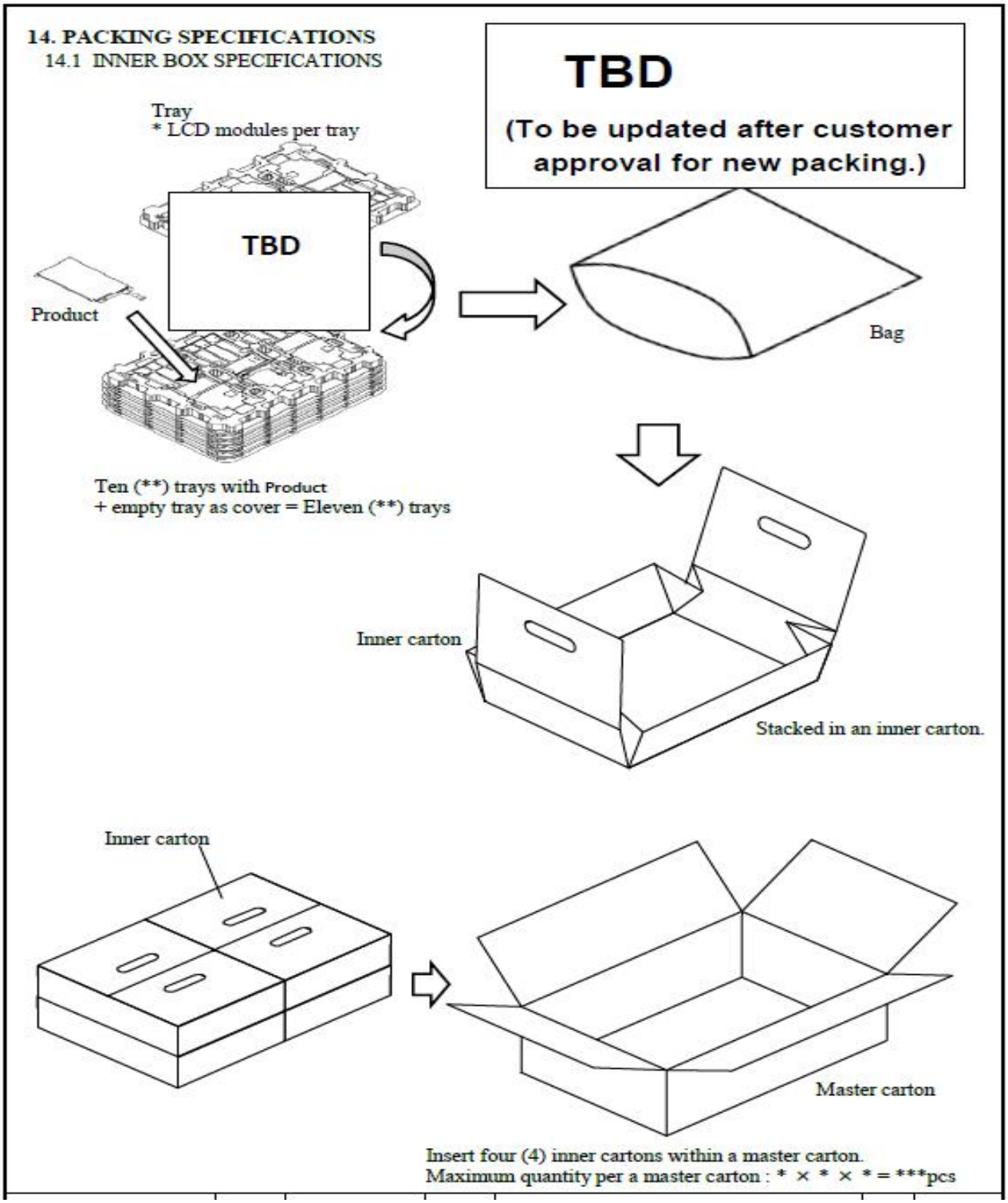
8. PACKAGE DRAWING