LCD MODULE

SPECIFICATION

Model:	UE040WV-RH30-A120A
Version:	V1.0
Date:	20221115

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Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20221115	Preliminary release	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：MIPI
3) Driver IC：GC9503V；TP IC：FT6336U
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode： Normally black, Transmissive
8) Pixel Density：169 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	4.0	Inch	Diagonal
Resolution	480(W)*3(RGB)*480(H)	Dots	-
Interface	MIPI	-	2 Lanes
Module Power Consumption	0.85	Watt	Typ.
Active Area	71.86(W)*70.18(H)	mm	-
Pixel pitch (W*H)	0.1497(W)*0.1462(H)	mm	-
Module Size (W*H*D)	84(W)*84(H)*3.11(D)	mm	-
Luminance	350	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	16.7M	Colors	24bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply4 voltage	VDD	-0.3	3.6	V	Note1
Power supply4 voltage	TPVCI	-0.3	3.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	℃	Note1,2
Storage temperature	T_{st}	-30	80	℃	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

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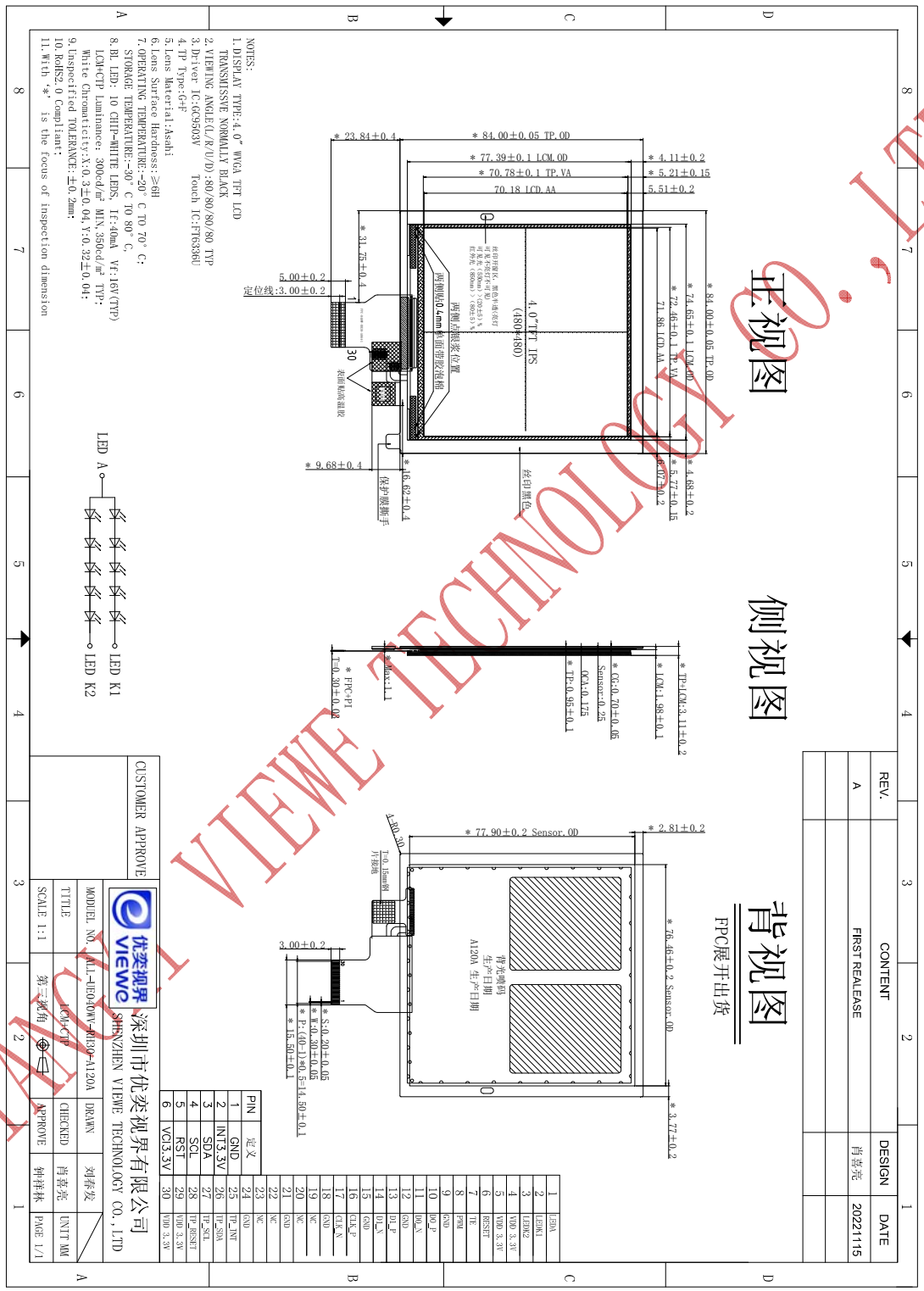
3. MECHANICAL DRAWING



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4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**LEDA**	P	Power supply for backlight anode
2	**LEDK1**	P	Power supply for backlight cathode
3	**LEDK2**	P	Power supply for backlight cathode
4-5	**VDD 3.3V**	P	Power supply for analog circuits
6	**RESET**	I	The signal will reset the LCM, Signal is active low.
7	**TE**	O	Tearing effect outputsignal. If not used, please let this pin open
8	**PWM**	I	This pin is connecting with the external LED driver
9	**GND**	P	Power Ground
10	**D0_P**	I/O	MIPI-DSI data lane 0 positive-end input pin
11	**D0_N**	I/O	MIPI-DSI data lane 0 negative-end input pin
12	**GND**	P	Power Ground
13	**D1_P**	I	MIPI-DSI data lane 1 positive-end input pin
14	**D1_N**	I	MIPI-DSI data lane 1 negative-end input pin
15	**GND**	P	Power Ground
16	**CLK_P**	I	MIPI-DSI clock lane positive-end input pin
17	**CLK_N**	I	MIPI-DSI clock lane negative-end input pin
18	**GND**	P	Power Ground
19-20	**NC**	-	No connected
21	**GND**	P	Power Ground
22-23	**NC**	-	No connected
24	**GND**	P	Power Ground
25	**TP_INT**	O	Interrupt signals for TP
26	**TP_SDA**	I/O	I2C data signal for TP
27	**TP_SCL**	I	I2C clock signals for TP
28	**TP_RESET**	I	The signal will reset the TP,Signal is active low
29-30	**VDD 3.3V**	P	Power supply for TP

I：Input；O：Output；P：Power

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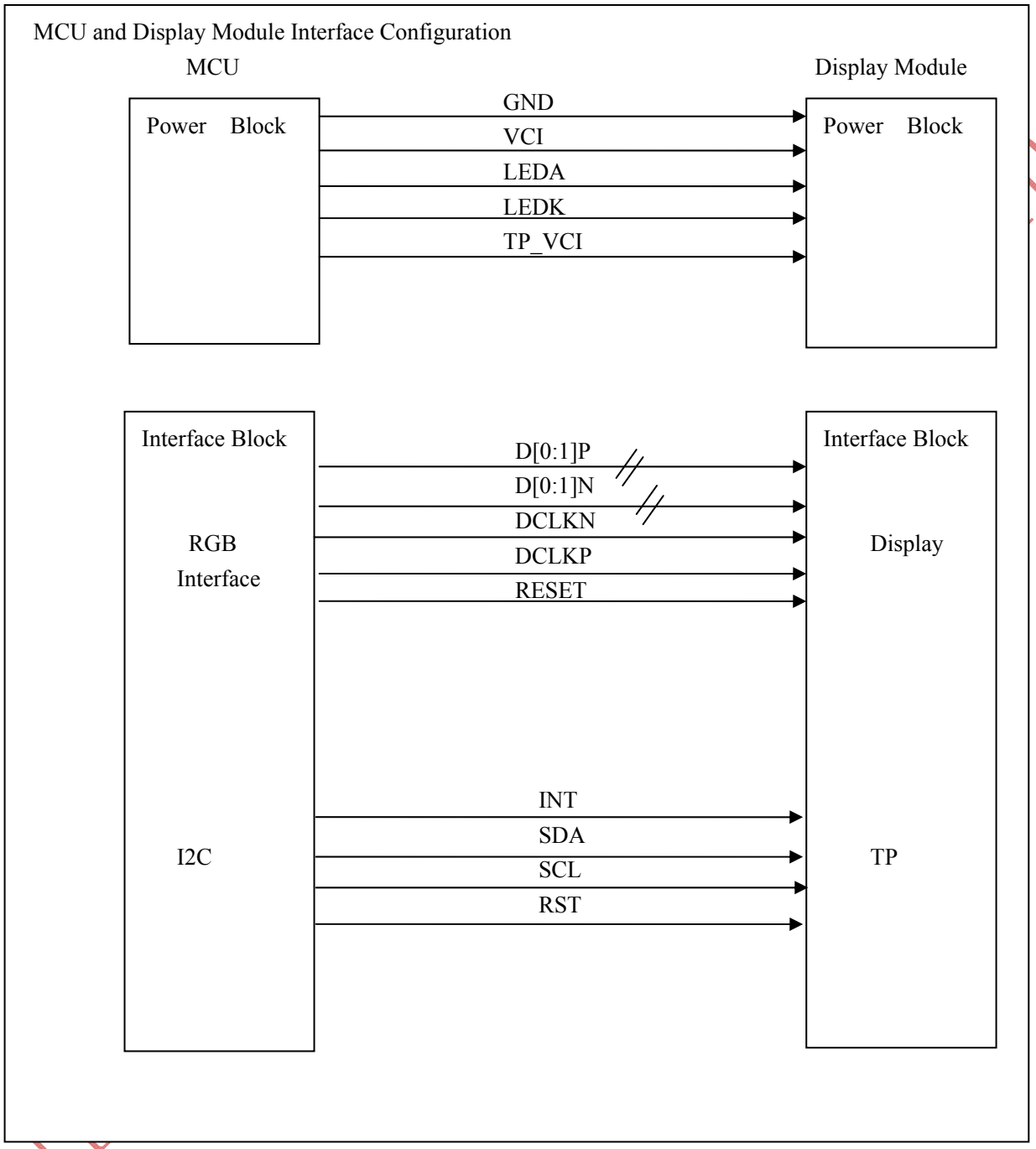
4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	VDD	3.3	3.3	3.6	V	-
Power Supply2 Voltage	TPVDD	2.8	3.3	3.3	V	-
Power Supply1 Current	I_{VDD}	-	50	-	mA	Note1
Power Supply4 Current	I_{TPVDD}	-	13	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7VDD	-	VDD	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3VDD	V	-
Panel Power Consumption	P_{VDD}	-	0.21	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.85	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

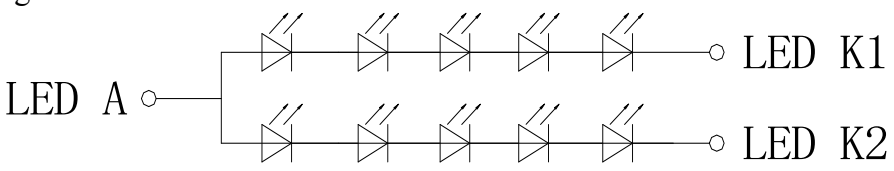
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	16	-	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.64	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			10		PCS	

(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module。For each LED ：
IF=20mA,VF=3.2V(Typ.)/3.4V(Max.),Ta=25℃。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



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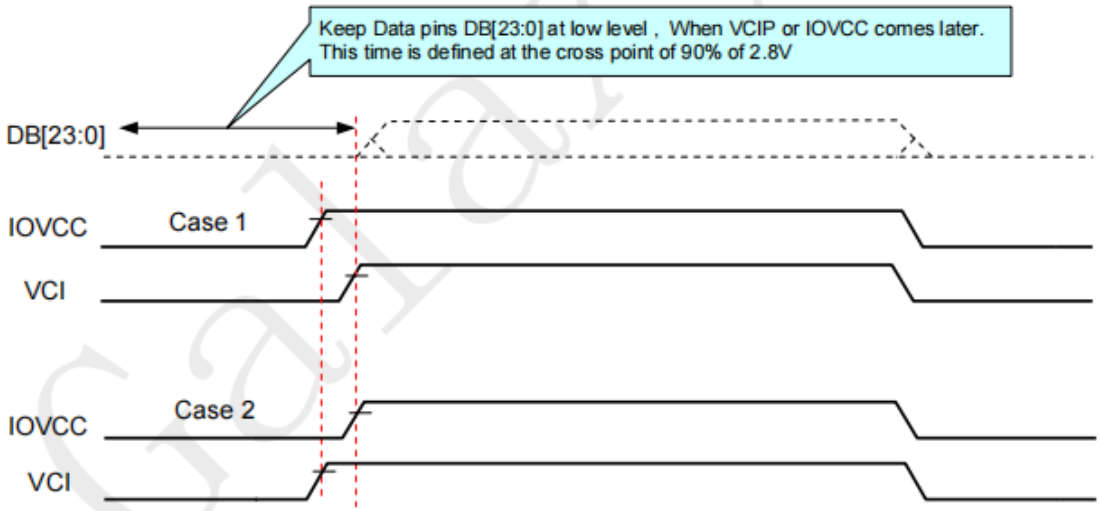
5.3 Power On/Off Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

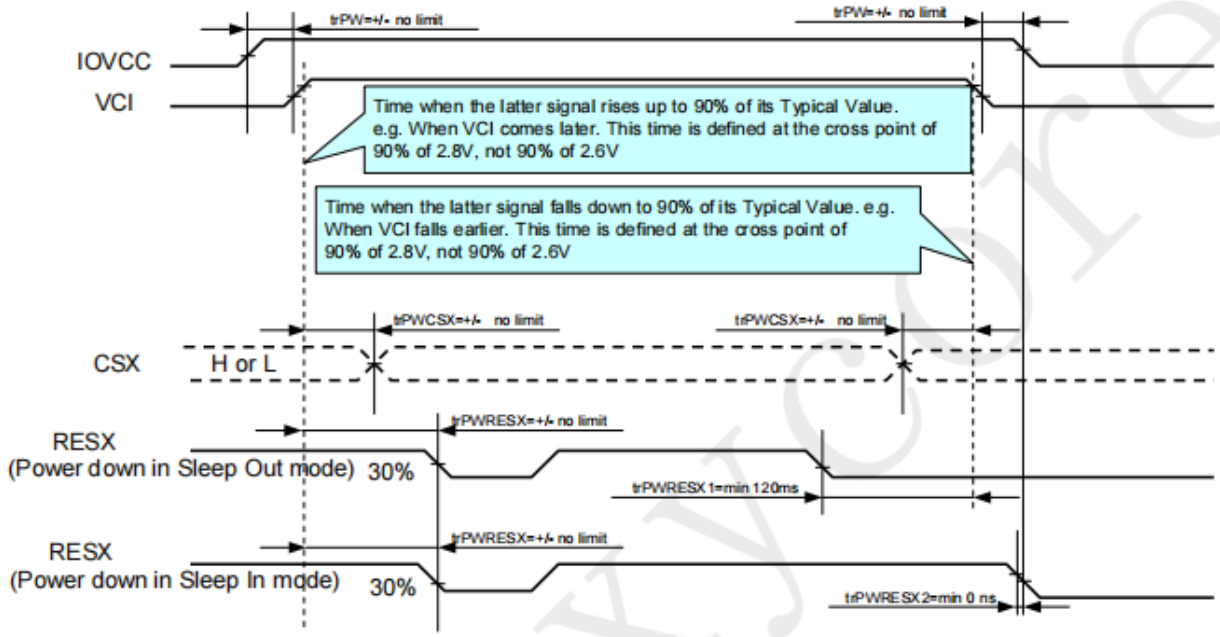
Note:

1. There will be no damage to GC9503V if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later



Case 1 –RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

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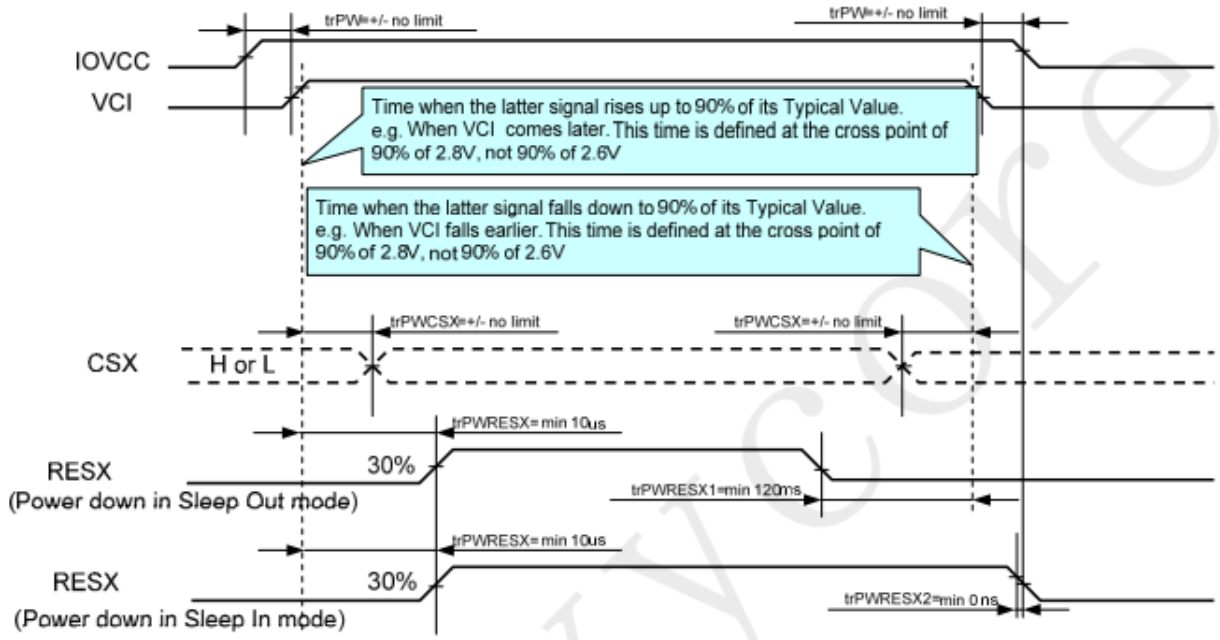
Case 2 – RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Figure 99 Case 2 – RESX line is held Low by Host at Power ON

Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

Uncontrolled power off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503V will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

TP

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

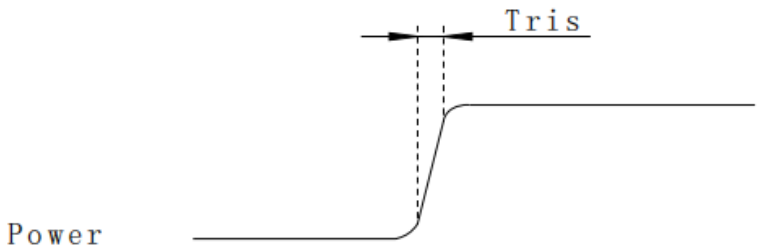


Figure 3-7 Power on time

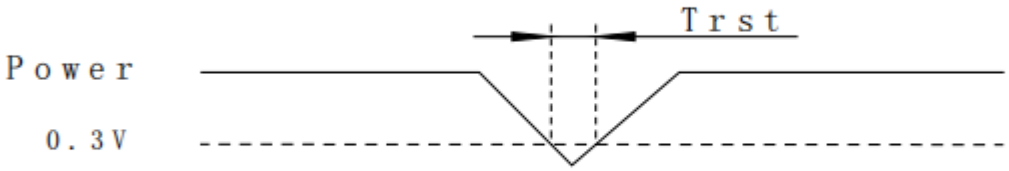


Figure 3-8 Power Cycle requirement

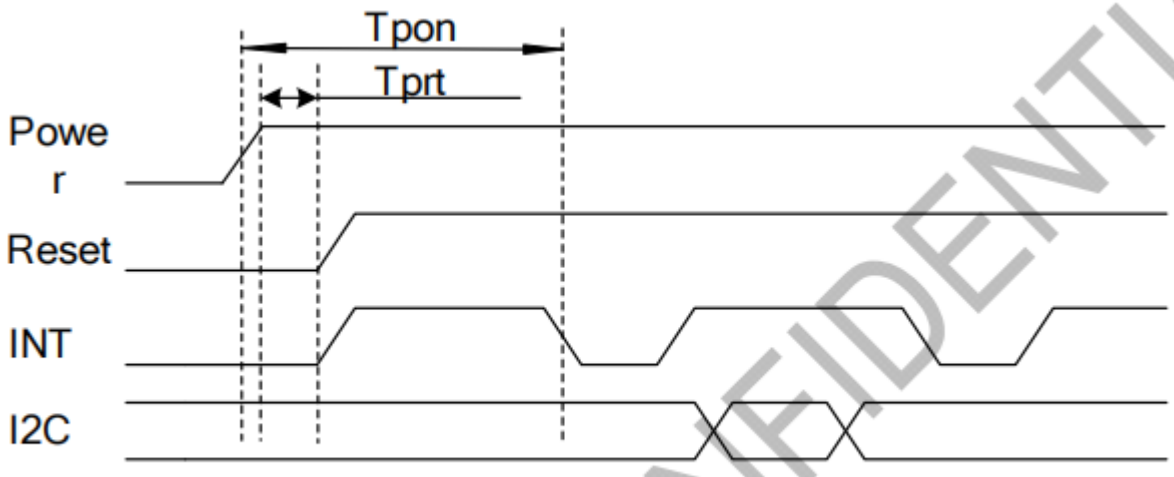


Figure 3-9 Power on Sequence

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Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

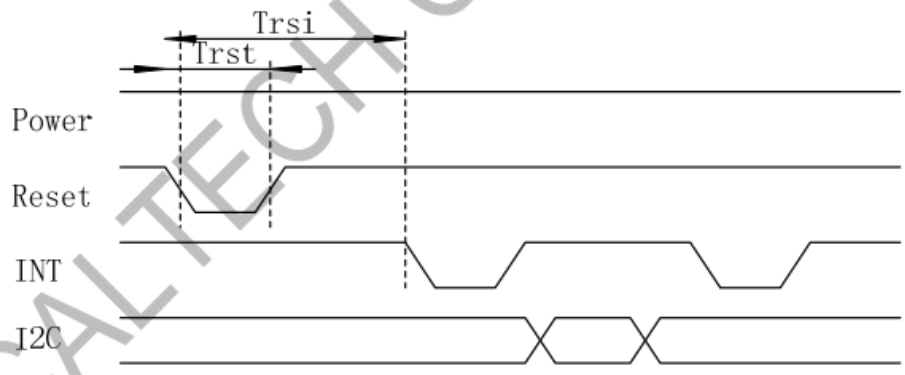

Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

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5.4 AC Characteristics

5.4.1 TP

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

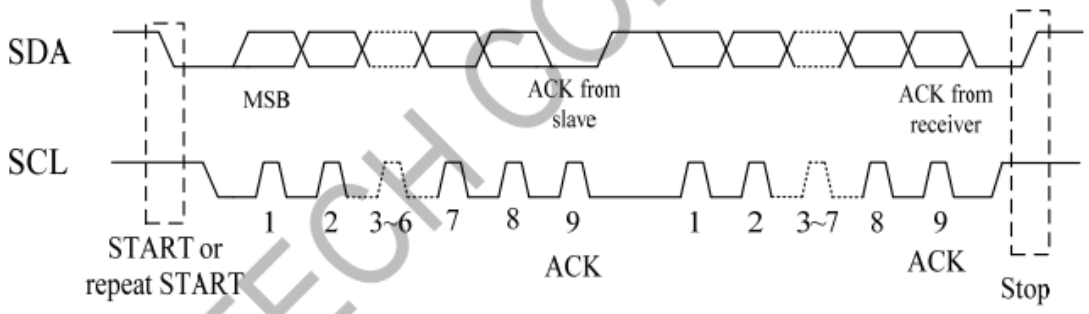

Figure 2-4 I2C Serial Data Transfer Format

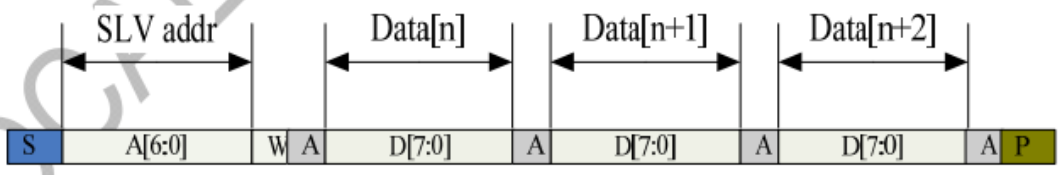

Figure 2-5 I2C master write, slave read

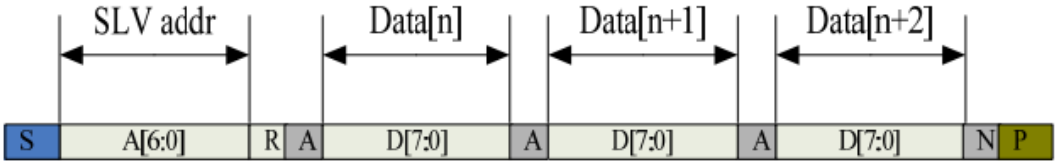

Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 3-4 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V； Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V； Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V； Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V； Ta=25℃	-	5	-	V	

High Speed Mode – Clock Channel Timing

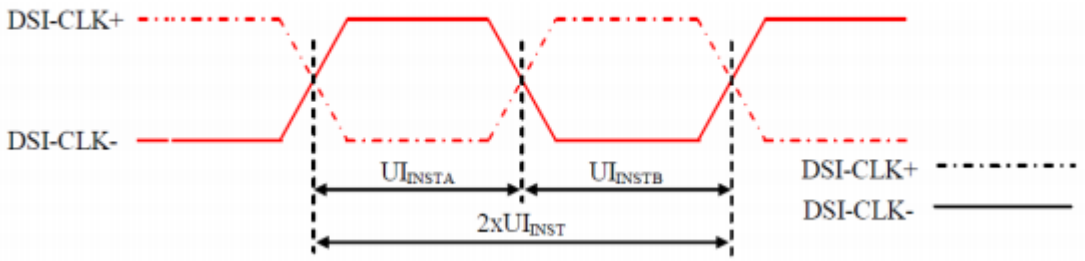

Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: UI = UI_{INSTA} = UI_{INSTB}

High Speed Mode – Data Clock Channel Timing

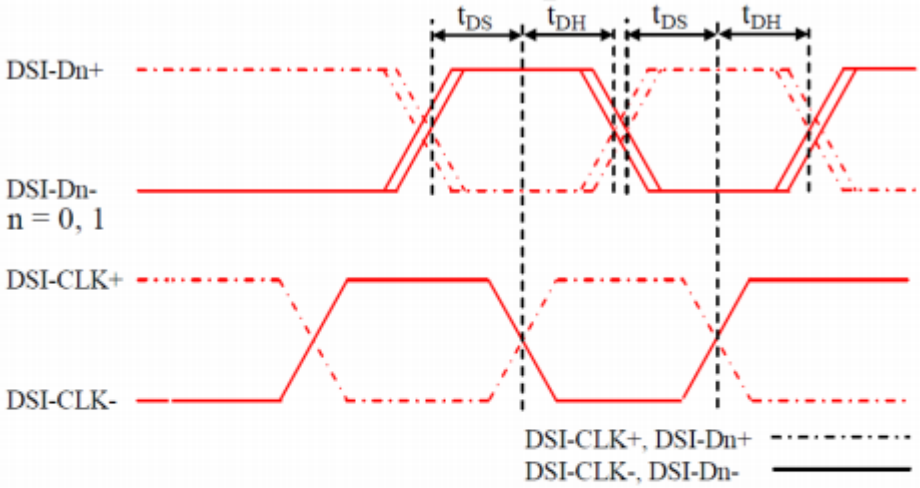

Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

High Speed Mode – Rise and Fall Timings

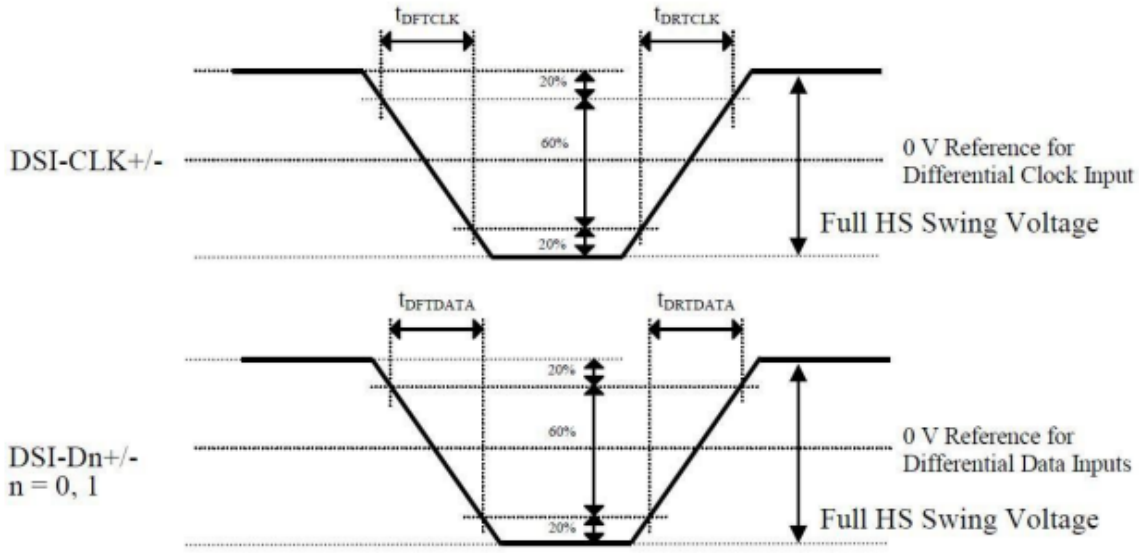

Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	-	-	150 (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note)	ps

Note:The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

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Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (GC9503V) sequence below.

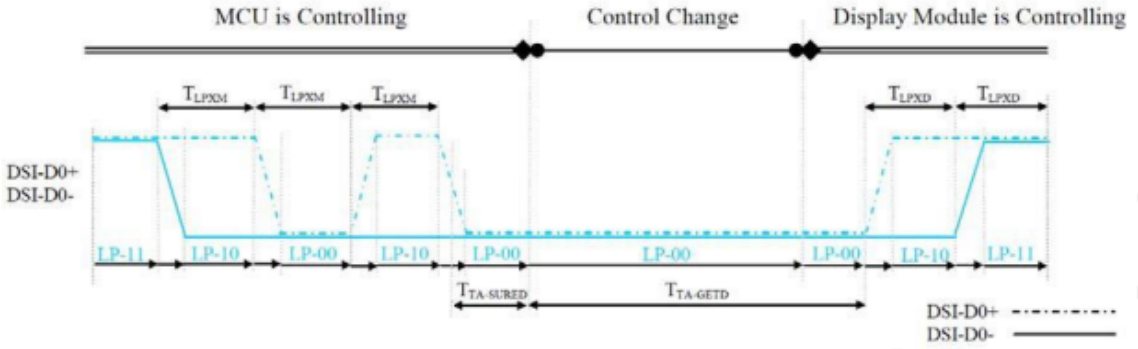

Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (GC9503V) to the MPU sequence below.

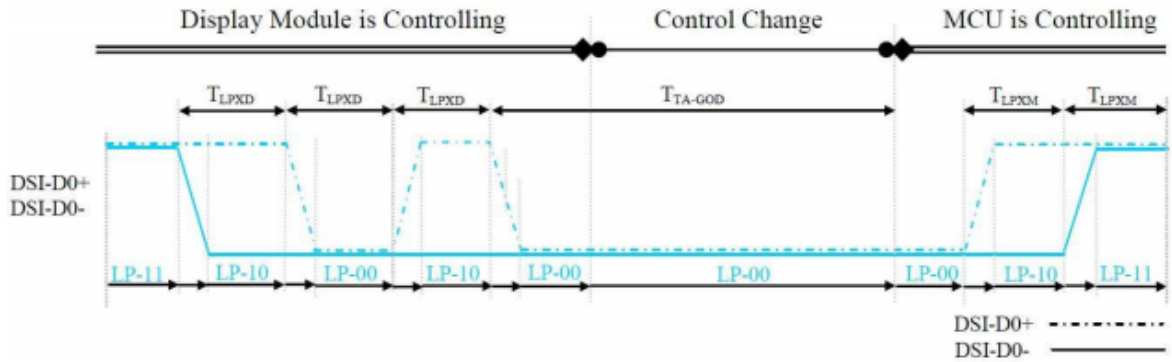

Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU 𝙸 Display Module (GC9503V)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (GC9503V) 𝙸 MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (GC9503V) starts driving	T_{LPXD}	$2\times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (GC9503V)	$5\times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

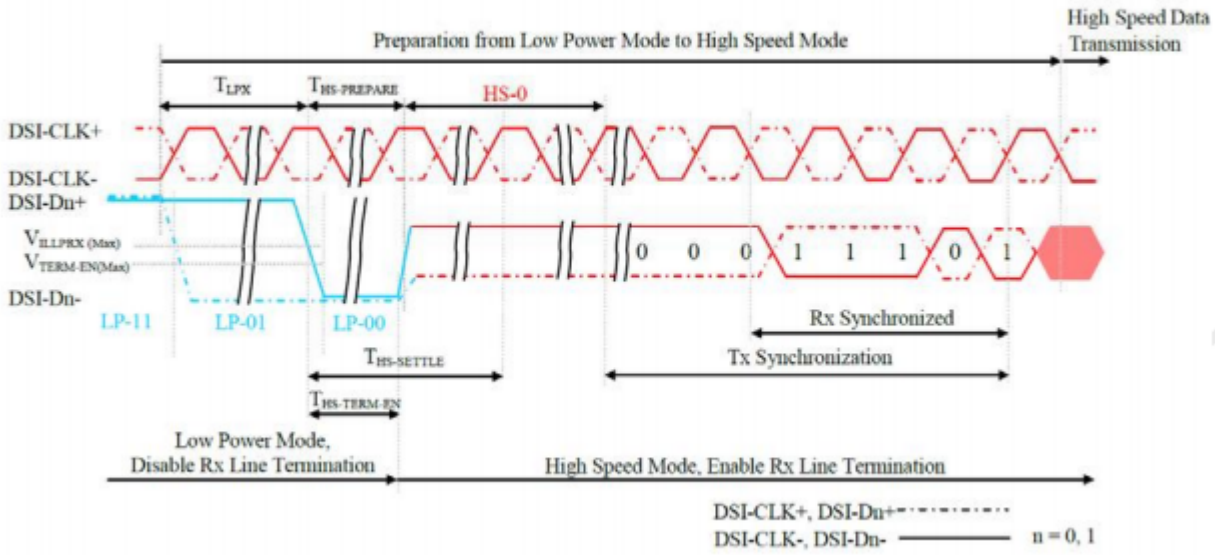

Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

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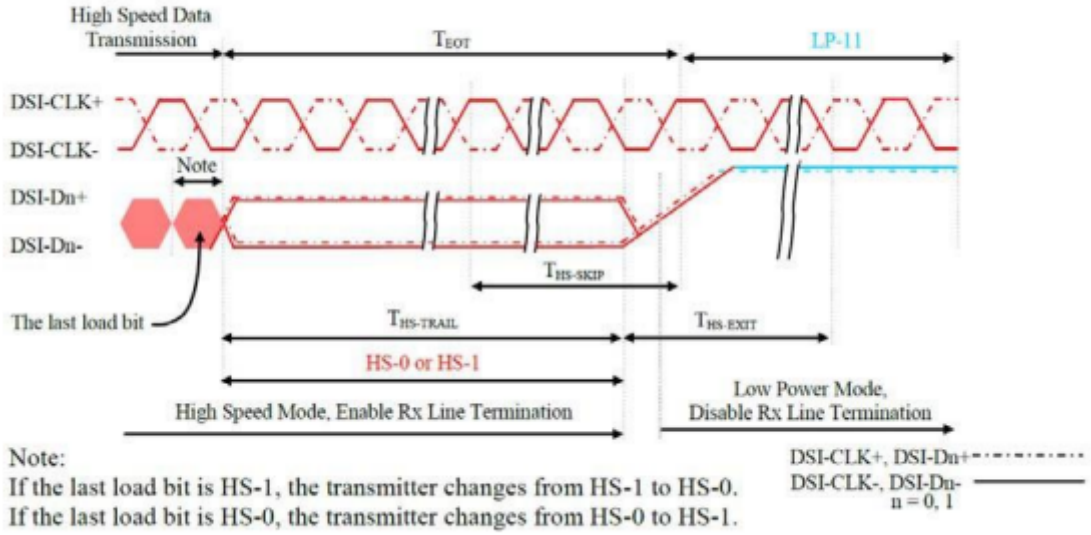
Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (GC9503V) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

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DSI Clock Burst – High Speed Mode to/from Low Power Mode

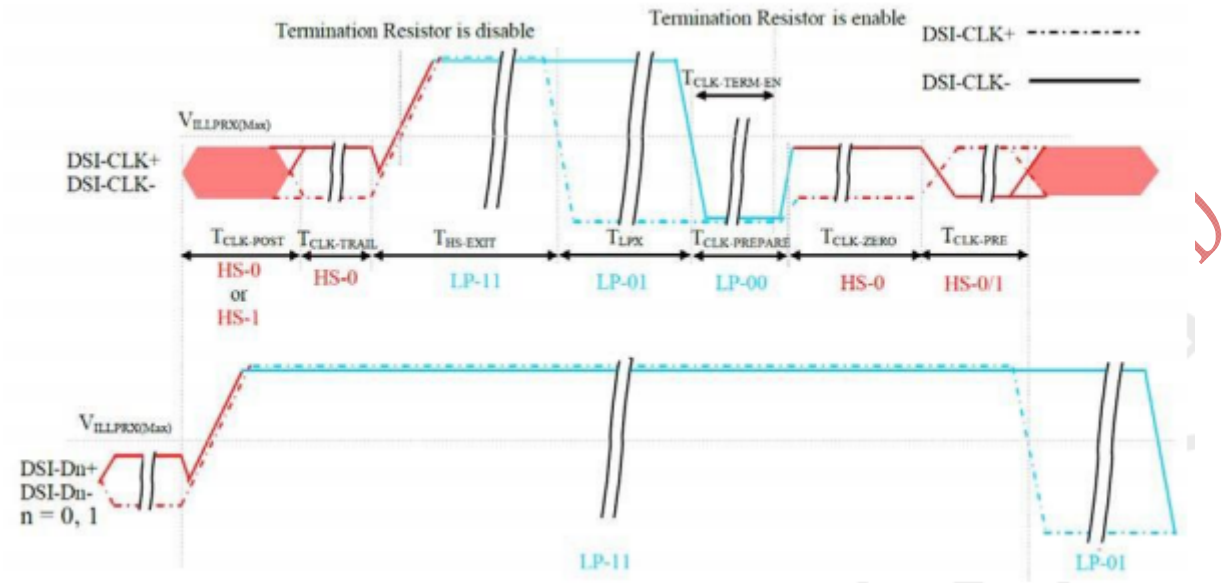

Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

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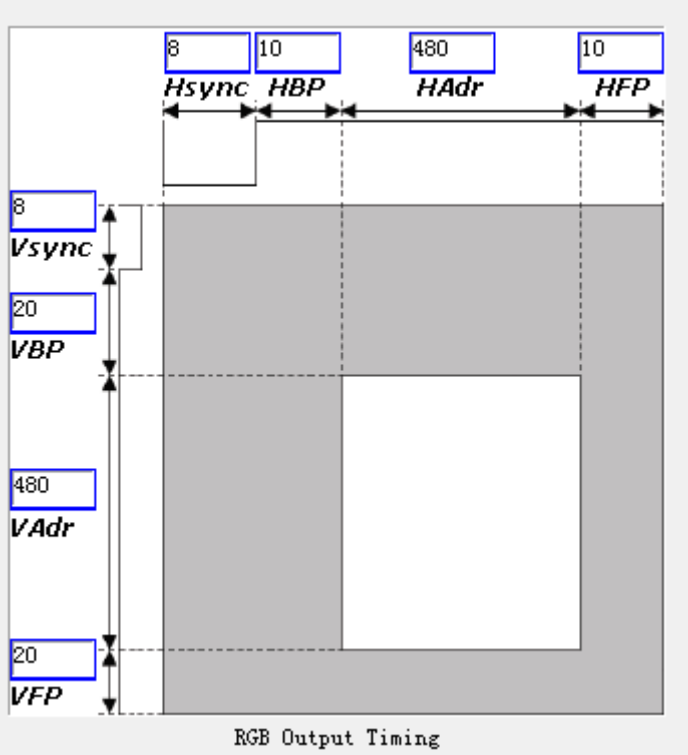
5.5 Timing Diagram



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6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	640	800	-	-	Note(4)
NTSC Ratio	S	θ =0°	55	60	-	%	Note(7)
Luminance	L	θ =0°	300	350	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	-	80	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	30	40	ms	Note(2)
Color Coordination	W_X	θ = 0° (Center) Normal viewing angle B/L On	-0.04	0.3	+0.02	NTSC (x,y)	Note(6)
	W_Y			0.32			
	R_X			0.639			
	R_Y			0.332			
	G_X			0.275			
	G_y			0.546			
	B_X			0.134			
	B_Y			0.128			
Viewing Angle	θ_L	C/R>10	-	80	-	Degree	Note(1)
	θ_R		-	80	-		
	θ_U		-	80	-		
	θ_D		-	80	-		

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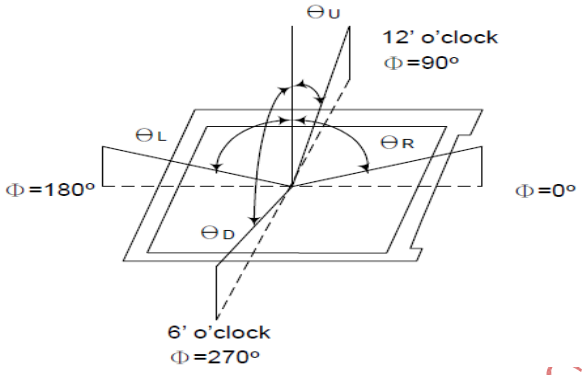
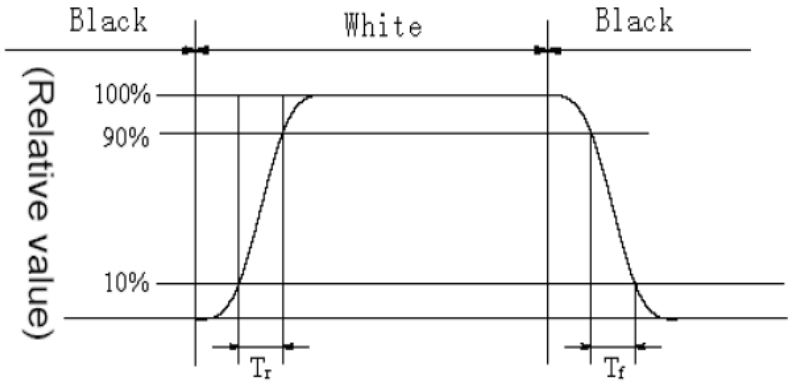
Test Conditions:

1. VDD=3.3V, I_F=40mA (Backlight current), the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

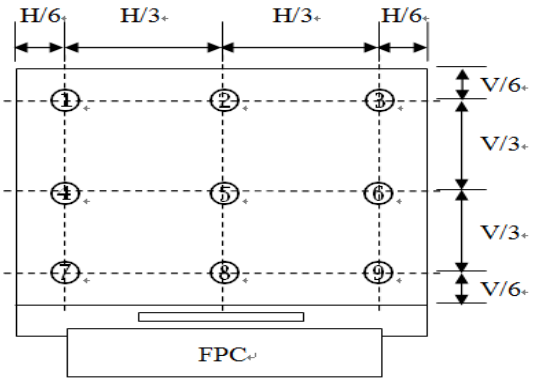


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

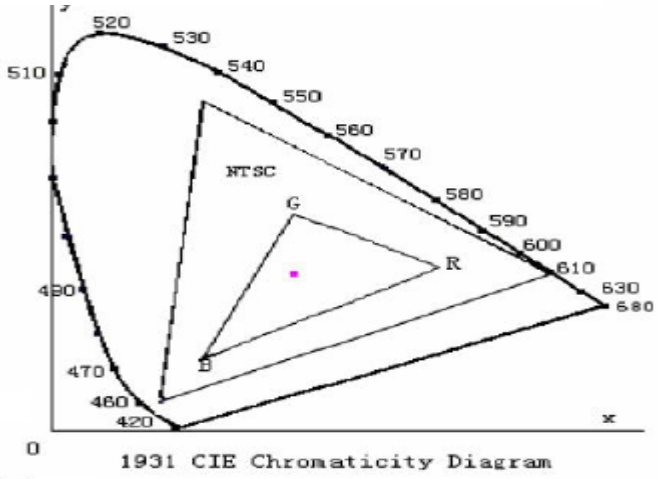
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

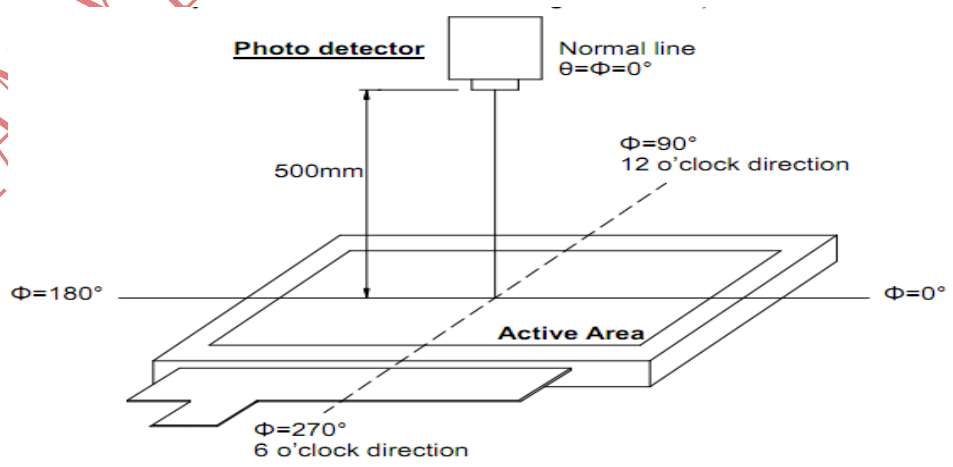
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min ⇆+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

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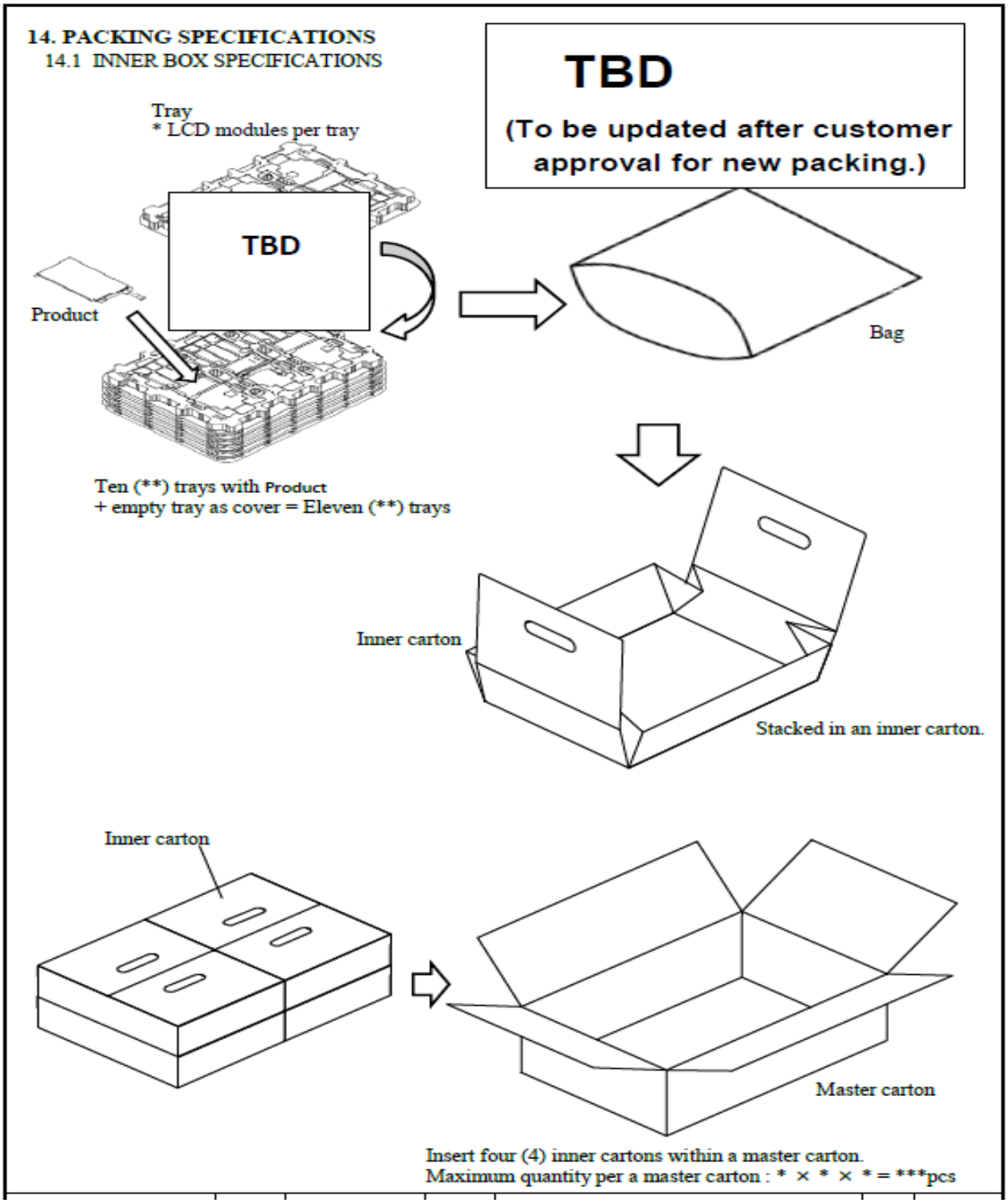
9. PACKAGE DRAWING