LCD MODULE

SPECIFICATION

Model:	UE040WV-RH40-A075B
Version:	V1.2
Date:	20220720

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Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20210521	Preliminary release	All
V1.1	20220112	Fix Color Coordination	
V1.2	20220720	Change mechanical drawing(ADD AF)	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：3 Wire SPI+16 Bits RGB
3) Driver IC：GC9503；TP IC：FT6336U
4) Operation Temperature：-20~60℃
5) Storage Temperature：-30~70℃
6) Backlight Type：White LED
7) Display mode： Normally black,
8) Pixel Density：169 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	4.0	Inch	Diagonal
Resolution	480(W)*3(RGB)*480(H)	Dots	-
Interface	3 Wire SPI+16 Bits RGB	-	-
Module Power Consumption	0.824	Watt	Typ.
Active Area	71.86(W)*70.18(H)	mm	-
Pixel pitch (W*H)	0.1497(W)*0.1462(H)	mm	-
Module Size (W*H*D)	83.6(W)*83.6(H)*3.23(D)	mm	-
Luminance	250	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	262K	Colors	18 Bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	VDD	-0.3	4.6	V	Note1
Power supply1 voltage	TP_VCI	-0.3	3.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	60	°C	Note1,2
Storage temperature	T_{st}	-30	70	°C	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,DGND=AVSS=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.
Temp. ＞60℃ , Absolute humidity shall be less than 90% RH.

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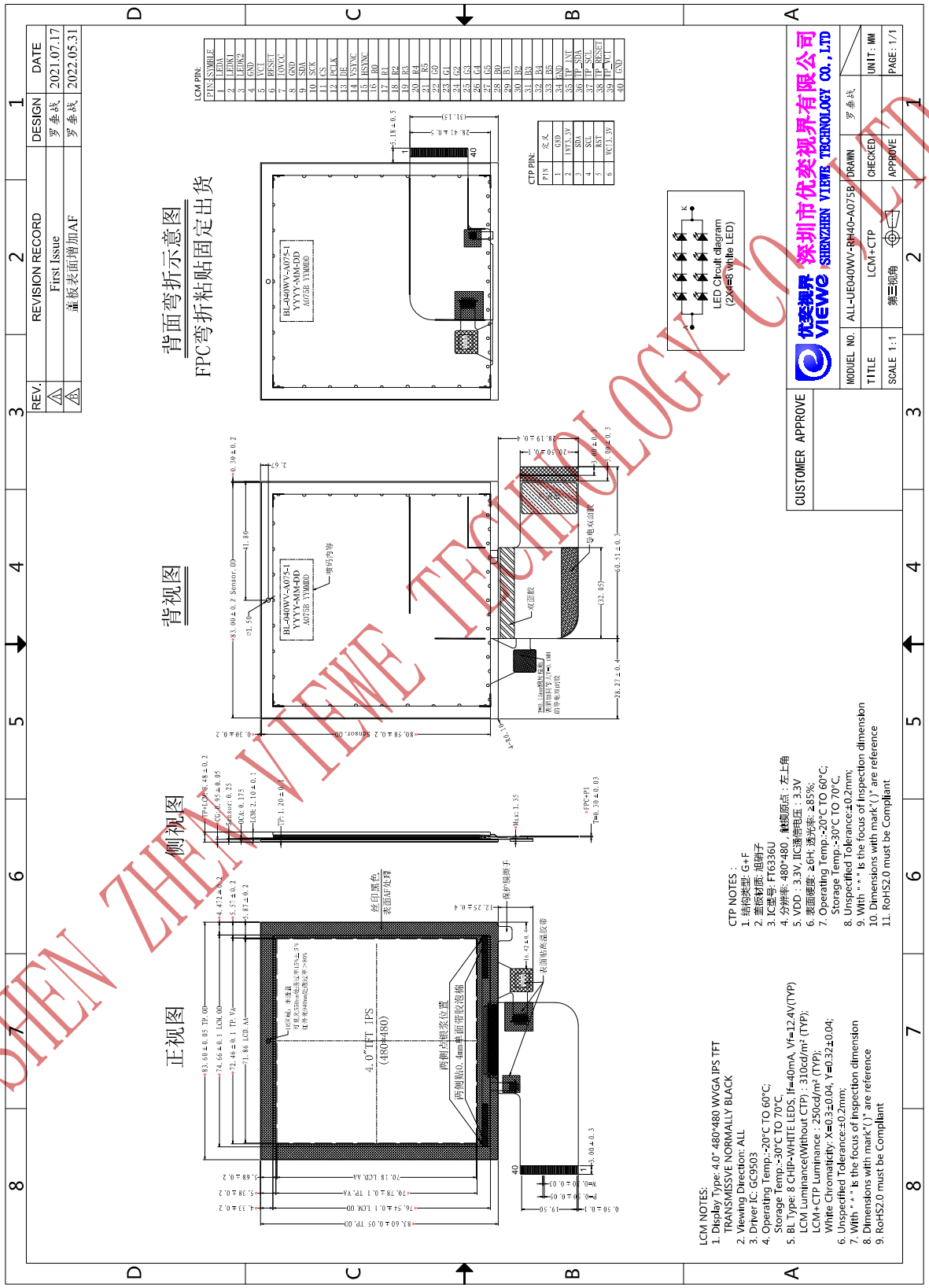
3. MECHANICAL DRAWING



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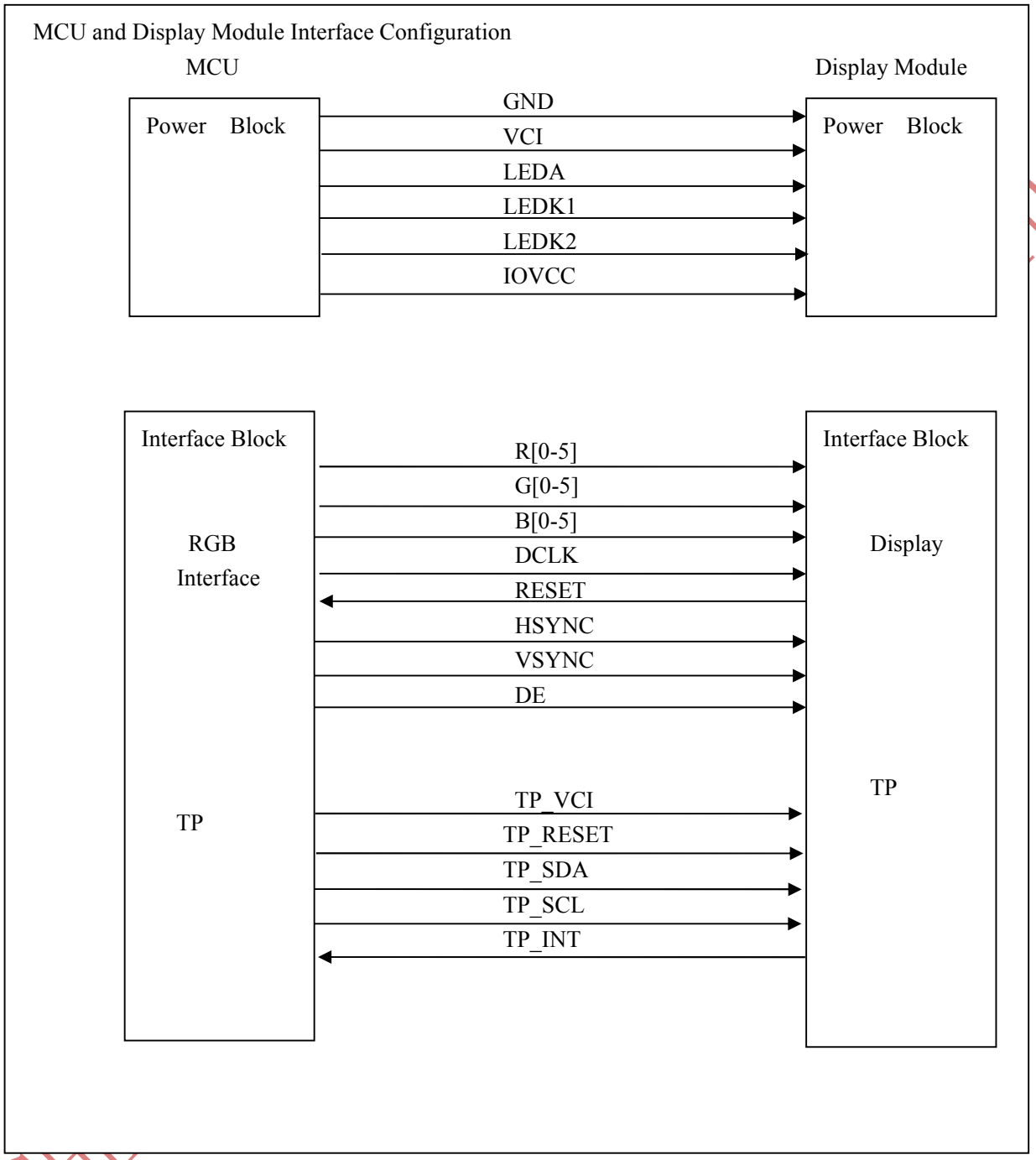
4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	LEDA	P	Power supply for backlight anode
2	LEDK1	P	Power supply for backlight cathode
3	LEDK2	P	Power supply for backlight cathode
4	GND	P	Power Ground
5	VCI	P	Power supply to the internal logic power regulator(3.3V)
6	RESET	I	The signal will reset the LCM, Signal is active low.
7	IOVCC	P	Power supply to the IO
8	GND	P	Power Ground
9	SDA	I/O	Serial in/out signal，for initial RGB I/F。 The data is applied on the rising edge of the SCL signal.
10	SCK	I	serial interface clock，for initial RGB I/F。
11	CS	I	Chip select input pin (“Low” enable)，for initial RGB I/F。
12	PCLK	I	Pixel clock input pin, Negative polarity
13	DE	I	Data input enable. Display access is enabled when DE is “H”
14	VSYNC	I	Vorizontal sync signal, Negative polarity
15	HSYNC	I	Hertical sync signal, Negative polarity
16-21	R0-R5	I	Red data input.
22-27	G0-G5	I	Green data input.
28-33	B0-B5	I	Blue data input.
34	GND	P	Power Ground
35	TP_INT	O	Interrupt signals for TP
36	TP_SDA	I/O	I2C data signals for TP
37	TP_SCL	I	I2C clock signals for TP
38	TP_RST	I	The signal will reset the TP, Signal is active low
39	TP_VCI	P	TP_VDD(2.8V) Power Supply for TP
40	GND	P	Power Ground

I：Input； O：Output； P：Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	VCI	2.5	3.3	3.3	V	
Power Supply2 Voltage	IOVCC	1.65	1.8	3.3		
Power Supply3 Voltage	TP_VCI	2.8	3.3	3.3	V	
Power Supply1 Current	I_{VDD}	-	50	-	mA	Note1
Power Supply2 Current	IOVCC		10			
Power Supply3 Current	I_{TP_VCI}	-	44	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3IOVCC	V	-
Panel Power Consumption	P_{VDD}	-	0.328	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	0.824	-	Watt	Note1,2

(Ta=+25°C, DGND=AVSS=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

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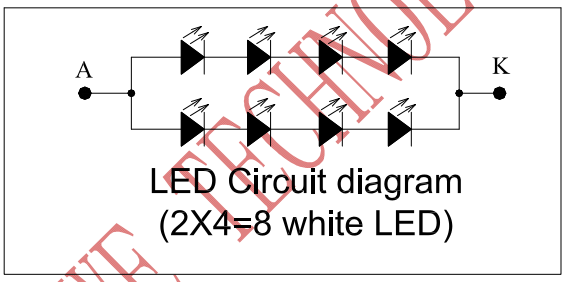
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	12.4	-	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.496	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			8		PCS	

(Ta=+25°C, DGND=AVSS=0V)

Note1: The LED driving condition is defined for

Note2:The "LED life time" is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



LED Circuit diagram
(2X4=8 white LED)

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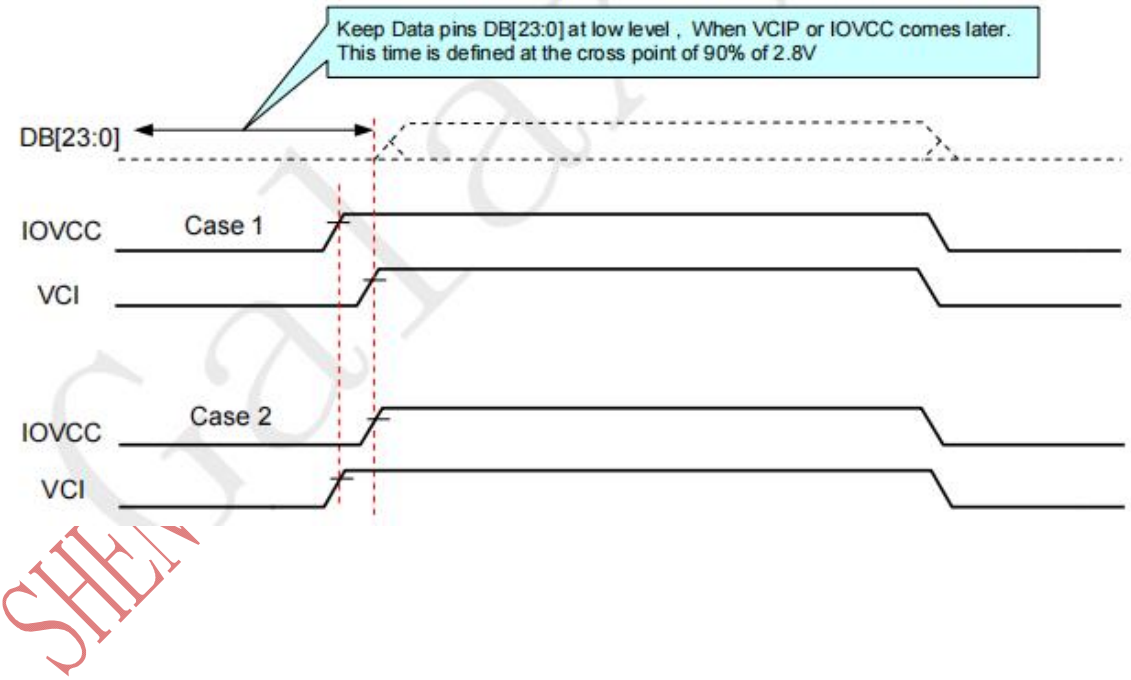
5.3 Power On/Off Sequence

IOVCC and VCI can be applied (or powered down) in any order. During the power off sequences, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down with minimum 120msec, and if LCD is in the Sleep In mode, VCI and IOVCC can be powered down with minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

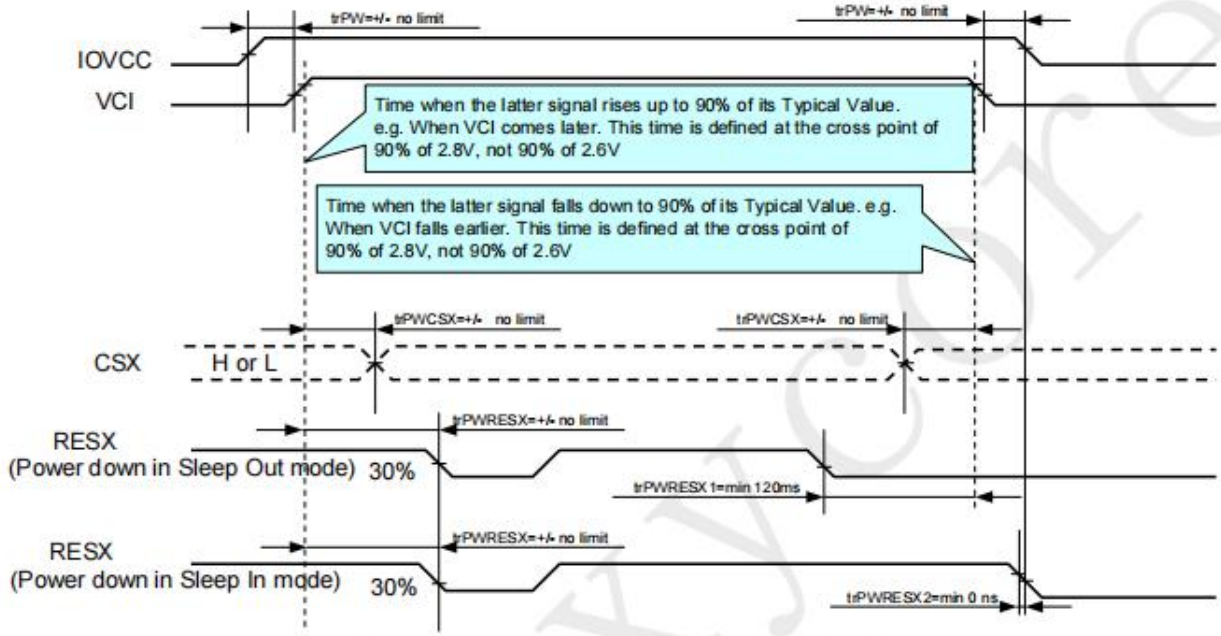
Note:

1. There will be no damage to GC9503V if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 7.1 and 7.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. Keep data pins DB[23:0] at low level, when VCIP or IOVCC comes later



RESX line is held High or Unstable by Host at Power ON

If the RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode

trPWRESX2 is applied to RESX falling in the Sleep In Mode

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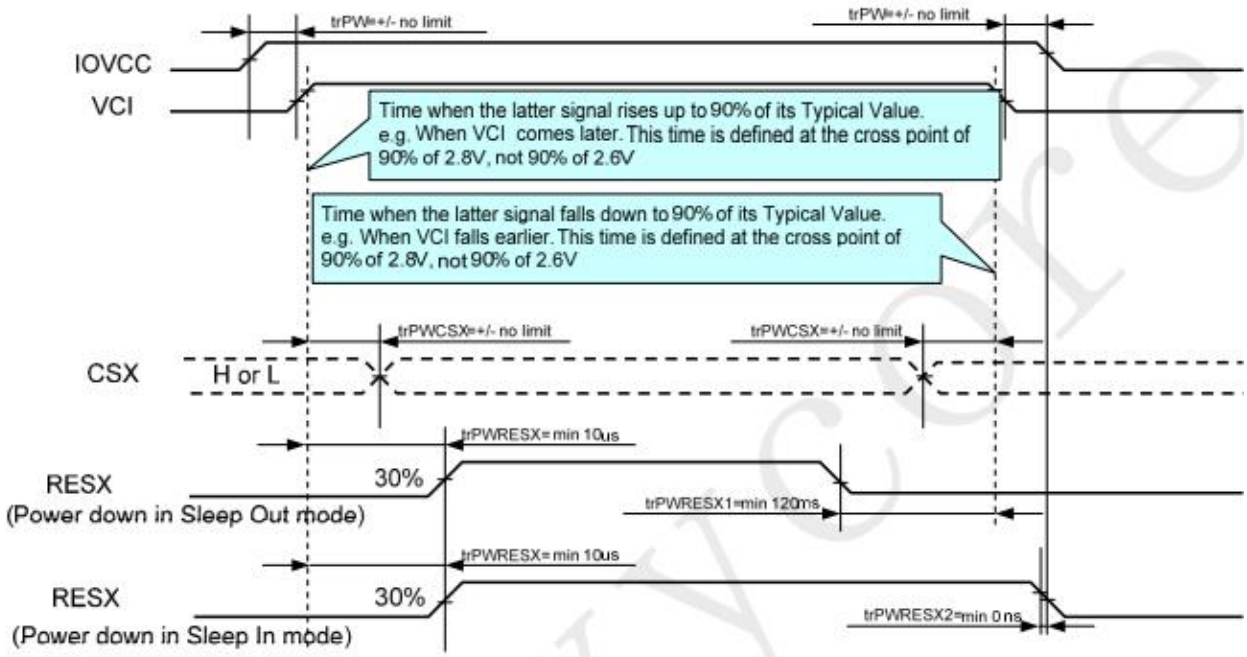
RESX line is held Low by Host at Power ON

If the RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and IOVCC have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode
trPWRESX2 is applied to RESX falling in the Sleep In Mode

Figure 99 Case 2 – RESX line is held Low by Host at Power ON

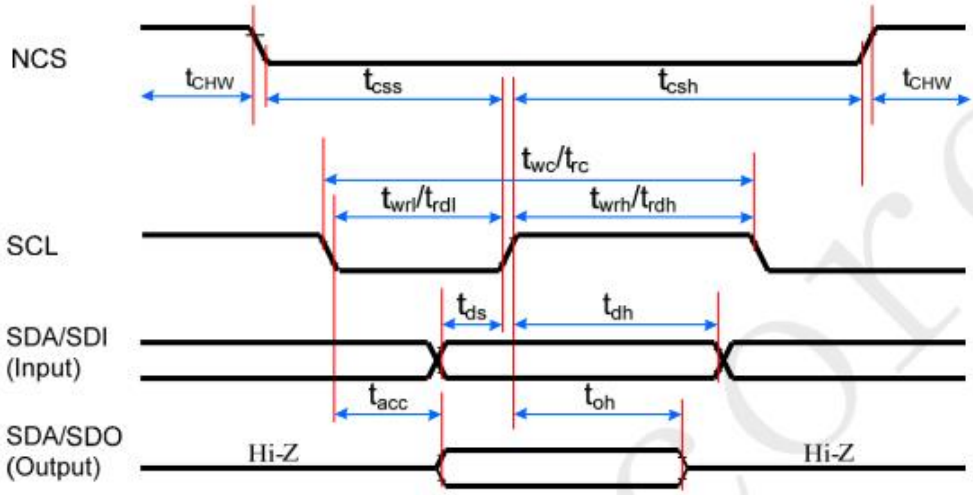
Note: 1. Unless otherwise specified, timings herein show cross point at 50% of signal power level.

Abnormal Power Off

The abnormal power off means a situation when e.g. there is removed a battery without the normal power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an abnormal power off event, GC9503V will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until “Power On Sequence” powers it up

5.4 Timing Characteristics

5.4.1 Timing for 3-Wire SPI Interface

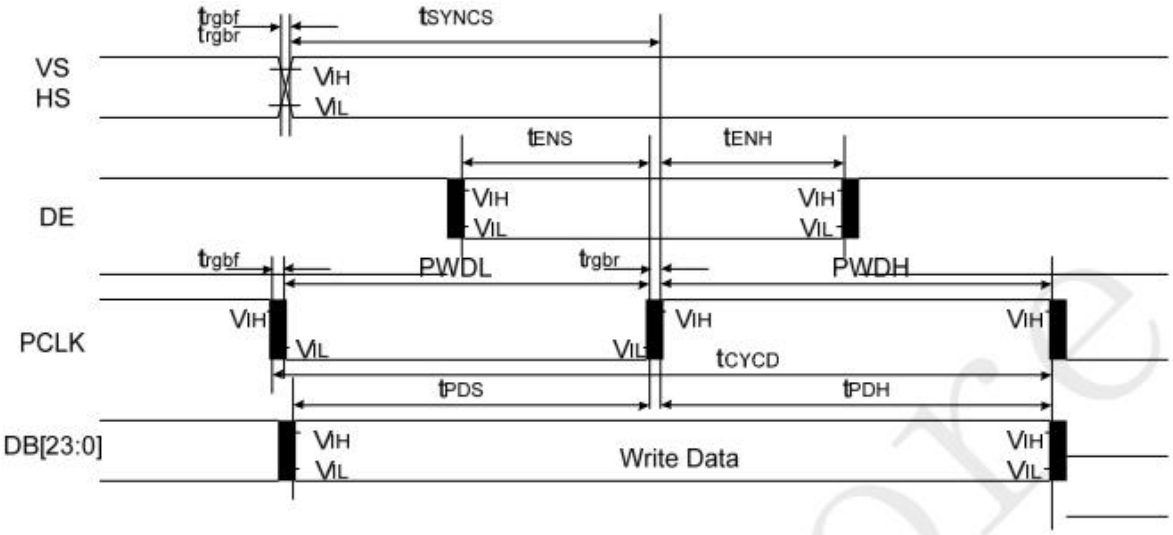


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	15	-	ns	
	tcsh	Chip select hold time (Read)	15	-	ns	
	tCHW	CS "H" pulse width	40	-	ns	
SCL	twc	Serial clock cycle (Write)	30	-	ns	
	twrh	SCL "H" pulse width (Write)	10	-	ns	
	twrl	SCL "L" pulse width (Write)	10	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
SDA/SDO (Output)	tacc	Access time (Read)	10	100	ns	For maximum CL=30pF
	toh	Output disable time (Read)	15	100	ns	For minimum CL=8pF
SDA/SDI (Input)	tds	Data setup time (Write)	10	-	ns	
	tdh	Data hold time (Write)	10	-	ns	

Note:

1. Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, T=10+/-0.5ns.
2. Does not include signal rise and fall times.

5.4.2 Timing for RGB Interface



Signal	Symbol	Parameter	min	max	Unit	Description
VS/ HS	t_{SYNCS}	VS/HS setup time	5	-	ns	24/18/16-bit bus RGB interface mode
	t_{SYNCH}	VS/HS hold time	5	-	ns	
DE	t_{ENS}	DE setup time	5	-	ns	
	t_{ENH}	DE hold time	5	-	ns	
DB[23:0]	t_{POS}	Data setup time	5	-	ns	
	t_{PDH}	Data hold time	5	-	ns	
PCLK	PWDH	PCLK high-level period	13	-	ns	
	PWDL	PCLK low-level period	13	-	ns	
	t_{CYCD}	PCLK cycle time	28	-	ns	
	t_{rgbr} , t_{rgbf}	PCLK,HS,VS rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.6V, VCI=2.5V to 3.6V, DGND=0V

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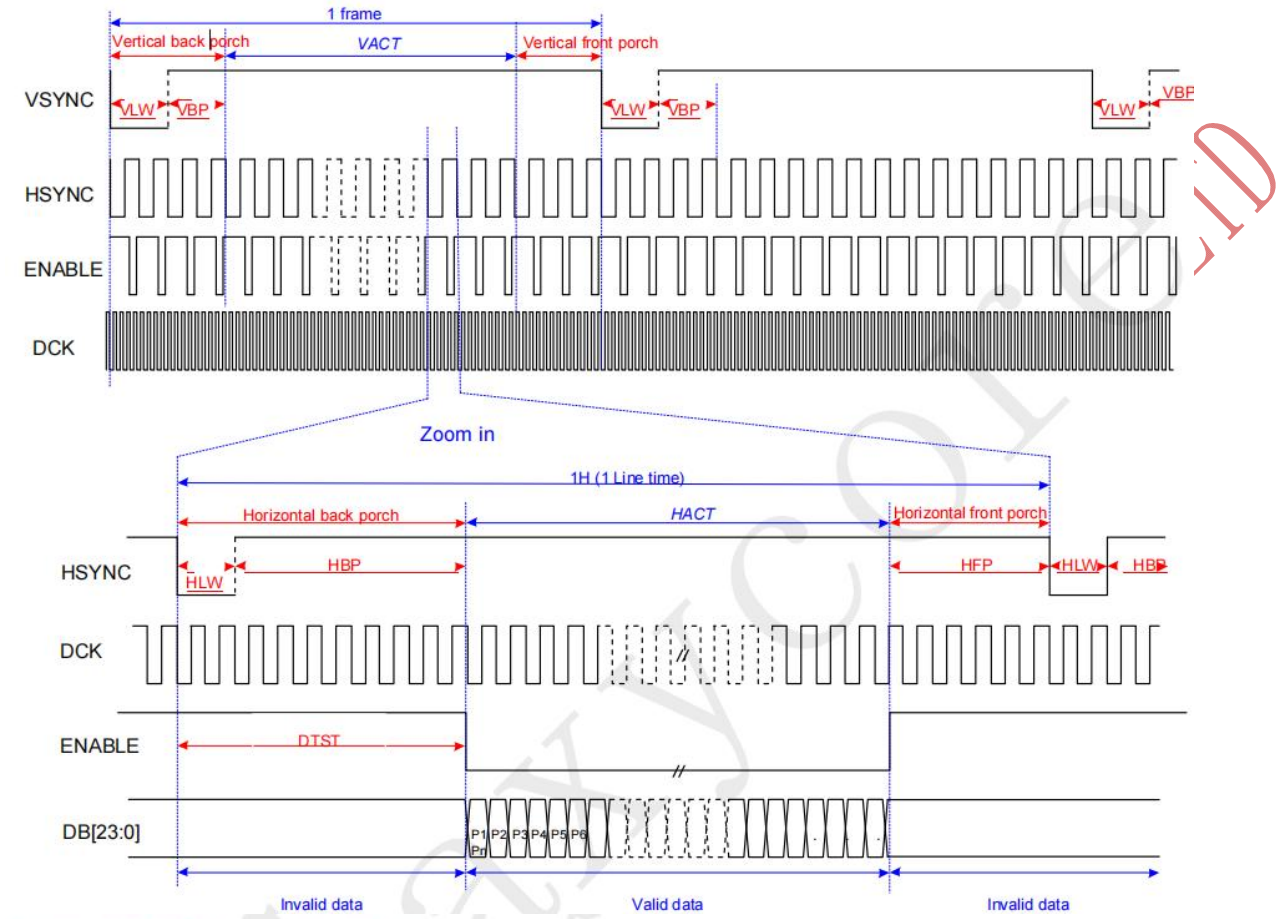
5.5 Timing Diagram



VLW : VSYNC Low pulse Width
HLW : HSYNC Low pulse Width
DTST : Data Transfer Startup Time
Pn : pixel 1, pixel 2···, pixel n.

Parameter	Symbol	Conditio	Min	Typ	Max	Units
Frame Rate	FR		54		6	fps
Horizontal Low Pulse width	HLW		1		-	DOTCL
Horizontal Back Porch	HBP		2		126	DOTCL
Horizontal Address	HACT			48		DOTCL
Horizontal Front Porch	HFP		2		-	DOTCL
Vertical Low Pulse width	VLW		1		126	Line
Vertical Back Porch	VBP		1		126	Line
Vertical Address	VACT				864	Line
Vertical Front Porch	VFP		1		255	Line
Data Clock	DCLK		16.		35.	MHz

Figure 12 DPI Interface Timing diagram[Note1,Note2]

6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	□= 0□	640	800	-	-	Note(4)
NTSC Ratio	S	□=0□	55	60	-	%	Note(7)
Luminance	L	□=0□	-	250	-	cd/m2	Note(5)
Luminance uniformity	Uw	□=0□	-	80	-	□	Note(3)
Response Time	TR+ TF	25 □C	-	30	40	ms	Note(2)
Color Coordination	Wx	□= 0□ (Center) Normal viewing angle B/L On	-0.04	0.3	+0.04	NTSC (x,y)	Note(6)
	Wy			0.32			
	Rx			0.639			
	Ry			0.332			
	Gx			0.275			
	Gy			0.546			
	Bx			0.134			
	By			0.128			
Viewing Angle	θ L	C/R□10	-	80	-	Degree	Note(1)
	θ R		-	80	-		
	θ U		-	80	-		
	θ D		-	80	-		

Test Conditions:

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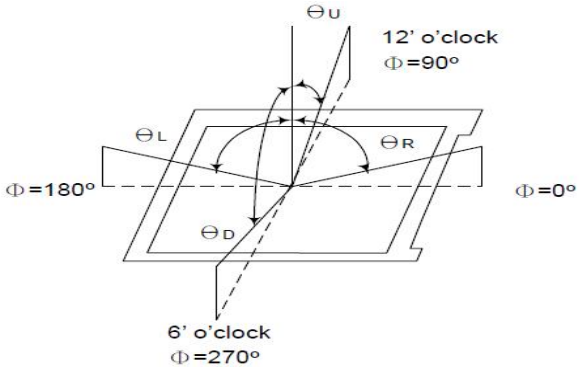
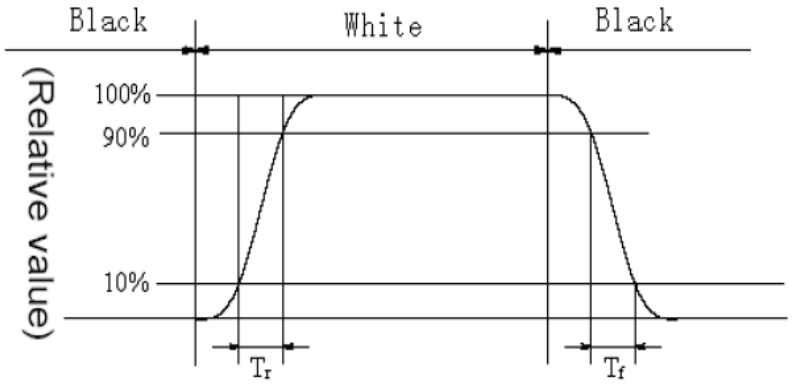
1. VDD=3.3V, I_F=20mA (Backlight current), the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR□10

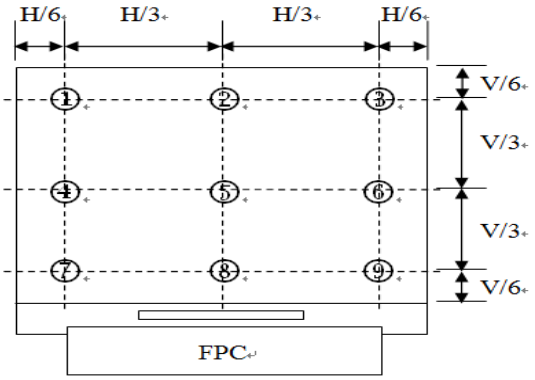


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

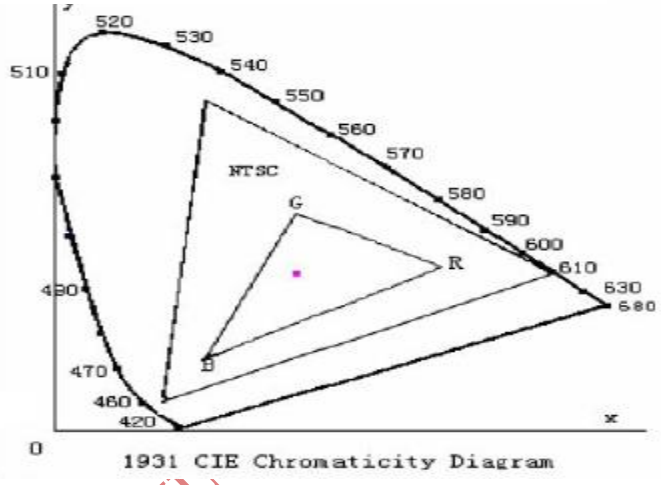
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

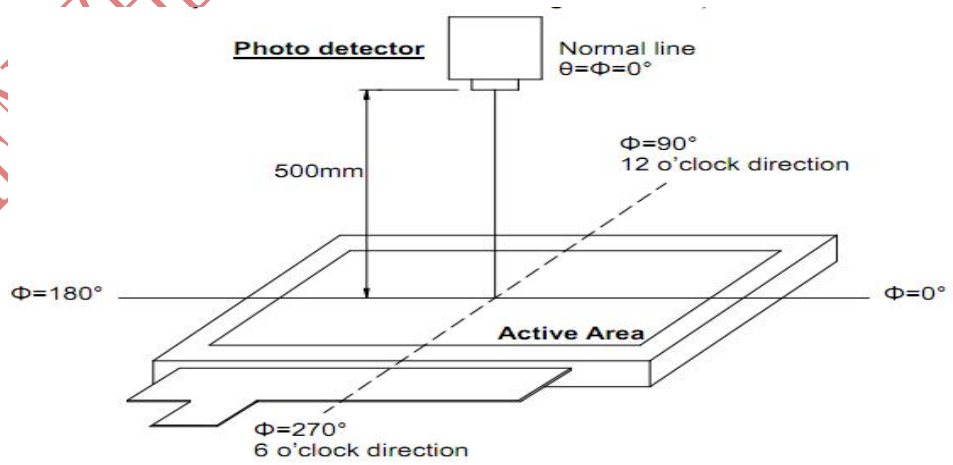
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+60°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min □+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
ESD	C=150PF,R=330 Ohm Air: ±8kv,5times(Center) Contact: ±4kv,5times(Center)	Note4

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

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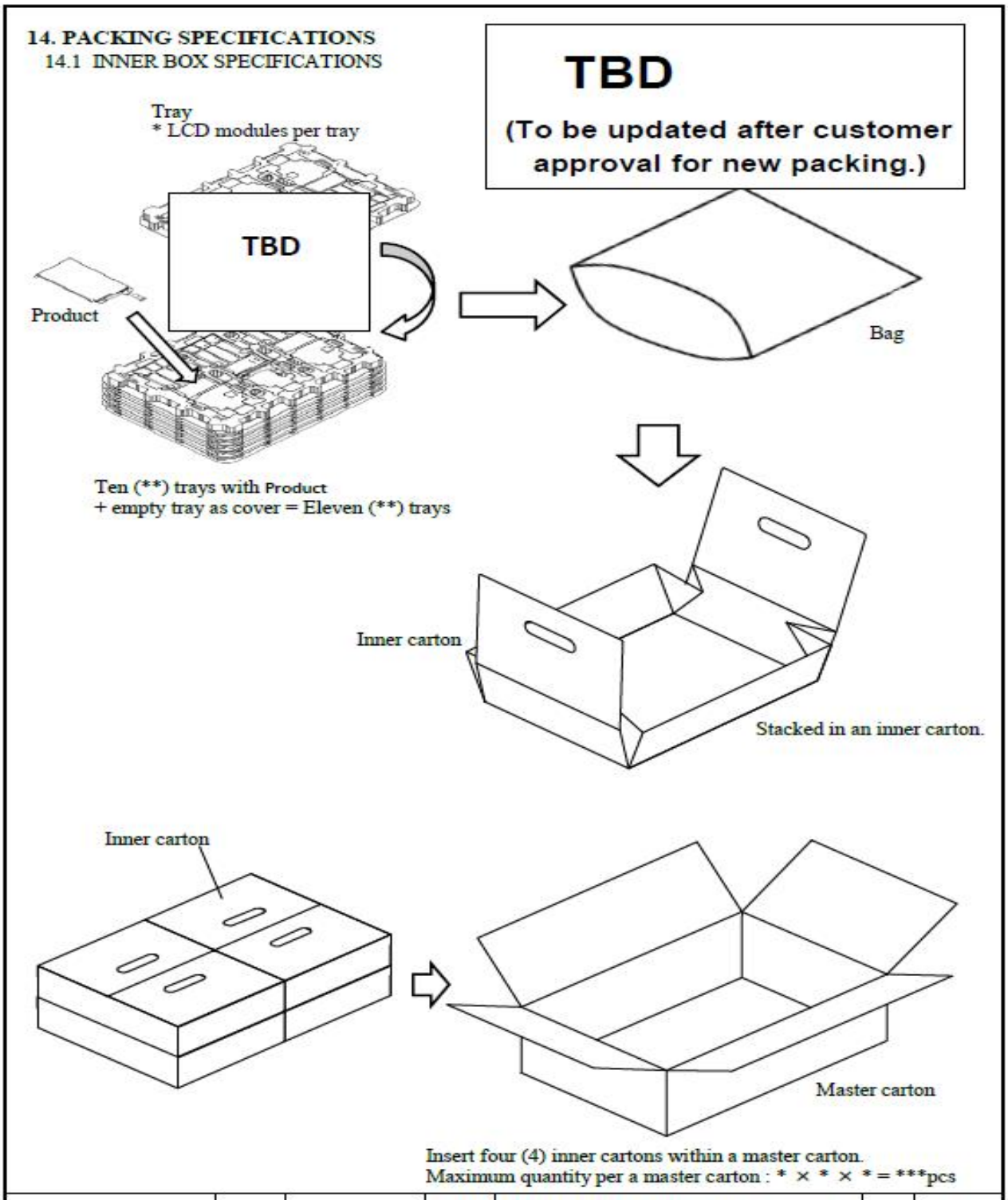
8. PACKAGE DRAWING