LCD MODULE

SPECIFICATION

Model:	UE101WU-RN30-A050C
Version:	V1.2
Date:	20230522

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Customer Confirmation 客户确认

Approved by	Notes

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Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20220630	Preliminary release	
V1.1	20220926	Change the CTP、FPC、B/L、TAPE etc...	
V1.2	20230522	Change the size of the cover glass	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode：MIPI
3) Driver IC：HX8279-D01；TP IC：GT9271
4) Operation Temperature：-10~50℃
5) Storage Temperature：-20~60℃
6) Backlight Type：White LED
7) Display mode： Normally black, Transmissive
8) Pixel Density：225 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	10.1	Inch	Diagonal
Resolution	1200(W)*3(RGB)*1920(H)	Dots	-
Interface	MIPI	-	4 Lanes
Module Power Consumption	TBD	Watt	Typ.
Active Area	135.36(W)*216.58(H)	mm	-
Pixel pitch (W*H)	0.0376(W)*0.1128(H)	mm	-
Module Size (W*H*D)	157.6(W)*240.0(H)*4.1(D)	mm	-
Luminance	400	cd/m^2	Typ.
Viewing Direction	All	O'clock	-
Display Color	16.7M	Colors	24bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	VDD	-0.3	3.6	V	Note1
Power supply2 voltage	IOVCC	-0.3	2.1	V	Note1
Power supply3 voltage	TP_VDD	-0.3	3.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-10	50	℃	Note1,2
Storage temperature	T_{st}	-20	60	℃	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.

Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

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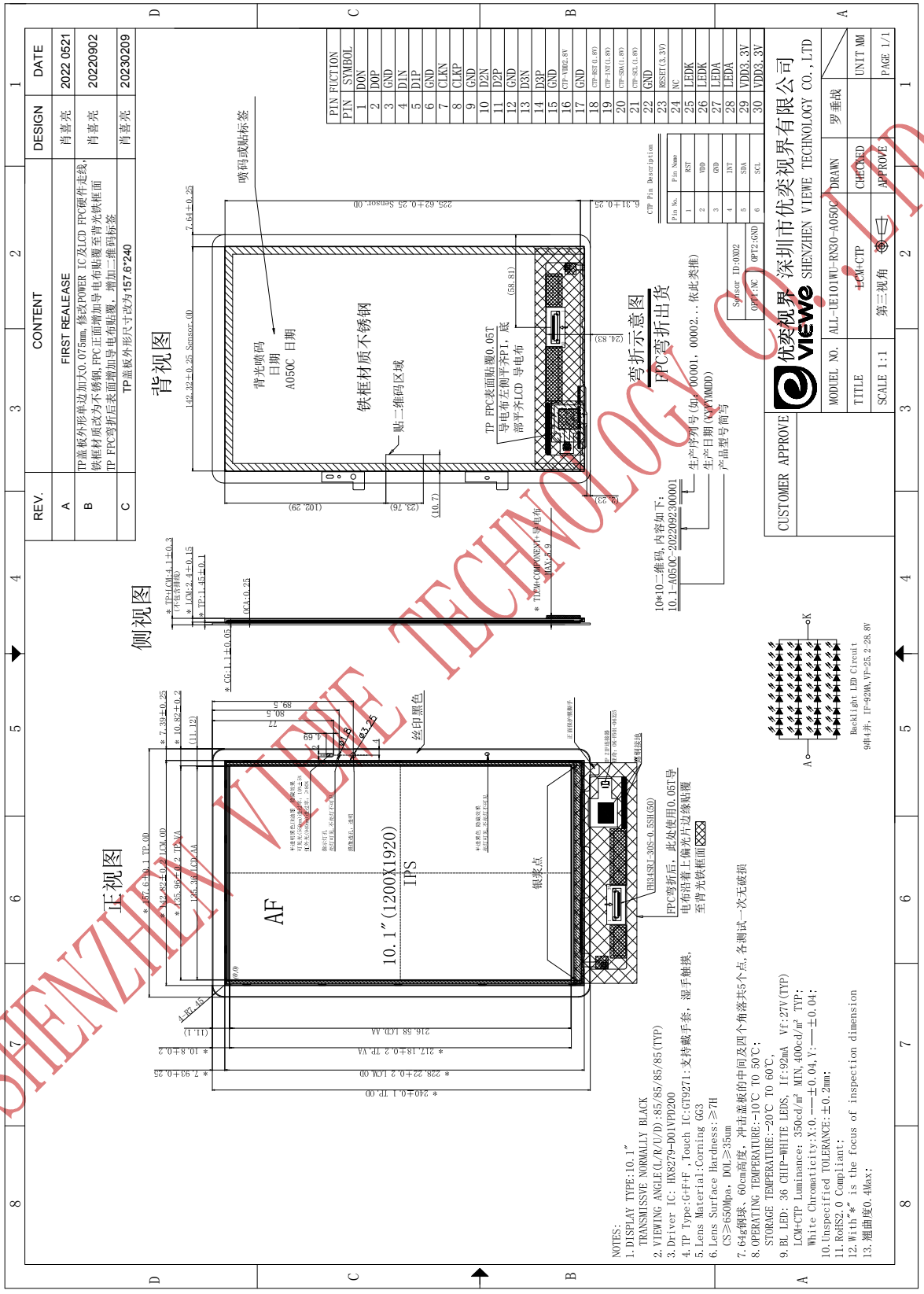
3. MECHANICAL DRAWING



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4. I/O CONNECTION & BLOCK DIAGRAM

4.1 I/O Connection

4.1.1 LCM I/O Connection

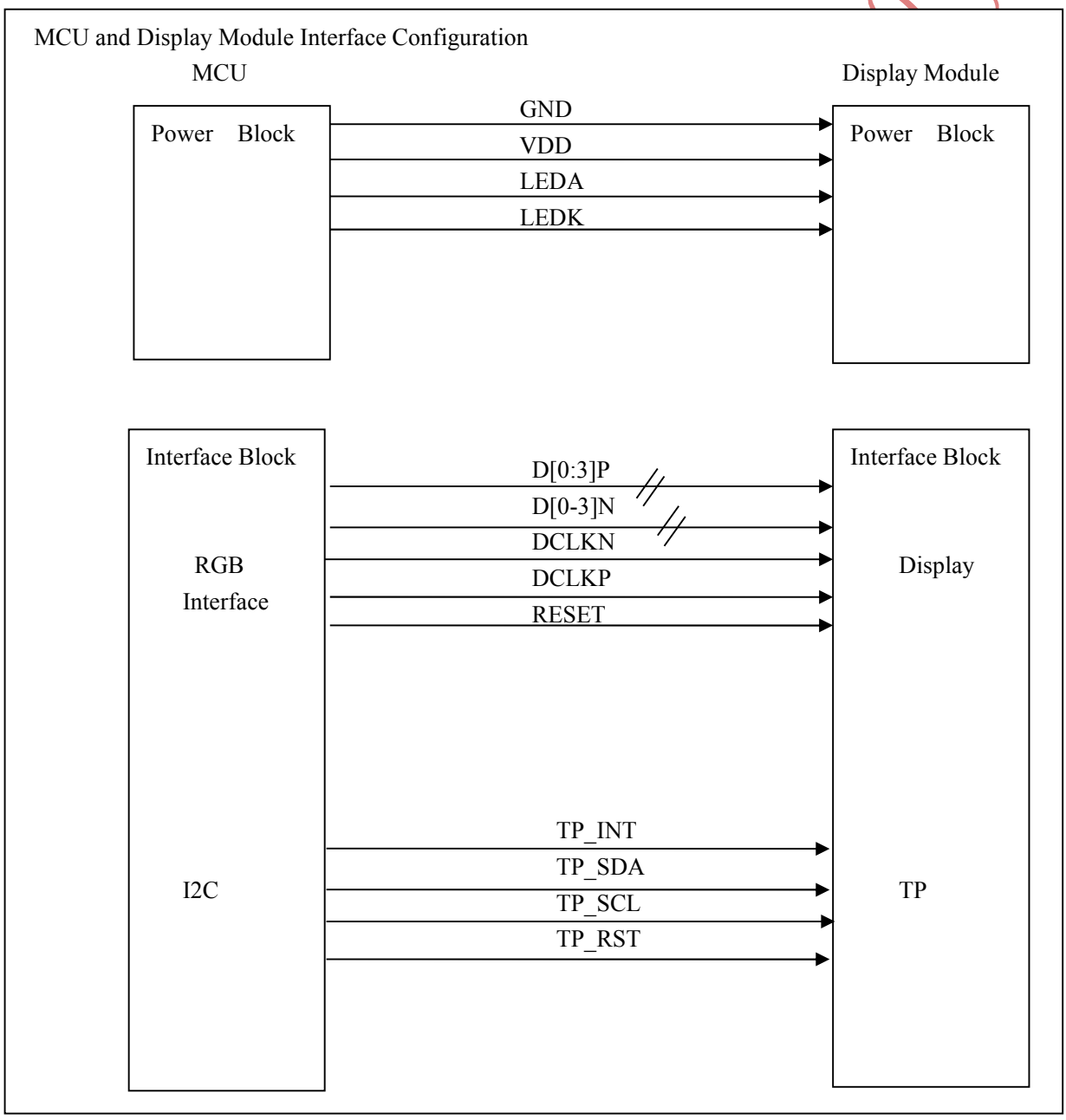
Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**D0N**	I	MIPI-DSI data lane 0 negative-end input pin
2	**D0P**	I	MIPI-DSI data lane 0 positive-end input pin
3	**GND**	P	I2C clock signal for CTP
4	**D1N**	I	MIPI-DSI data lane 1 negative-end input pin
5	**D1P**	I	MIPI-DSI data lane 1 positive-end input pin
6	**GND**	P	Power Ground
7	**CLKN**	I	MIPI-DSI clock lane negative-end input pin
8	**CLKP**	I	MIPI-DSI clock lane positive-end input pin
9	**GND**	P	Power Ground
10	**D2N**	I	MIPI-DSI data lane 2 negative-end input pin
11	**D2P**	I	MIPI-DSI data lane 2 positive-end input pin
12	**GND**	P	Power Ground
13	**D3N**	I	MIPI-DSI data lane 3 negative-end input pin
14	**D3P**	I	MIPI-DSI data lane 3 positive-end input pin
15	**GND**	P	Power Ground
16	**CTP-VDD2.8V**	P	Power supply for TP(2.8V)
17	**GND**	P	Power Ground
18	**CTP-RST(1.8V)**	I	The signal will reset the CTP,Signal is active low
19	**CTP-INT(1.8V)**	I	Interrupt signals for CTP
20	**CTP-SDA(1.8V)**	I	I2C data signal for CTP
21	**CTP-SCL(1.8V)**	I	I2C clock signal for CTP
22	**GND**	P	Power Ground
23	**RESET(3.3V)**	I	The signal will reset the LCM, Signal is active low
24	**NC**	-	-
25	**LEDK**	P	Power supply for backlight cathode
26	**LEDK**	P	Power supply for backlight cathode
27	**LEDA**	P	Power supply for backlight anode
28	**LEDA**	P	Power supply for backlight anode
29	**VDD3.3V**	P	Power supply (3.3V)
30	**VDD3.3V**	I	Power supply (3.3V)

I：Input；O：Output；P：Power

4.1.2 CTP I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**CTP-RST(1.8V)**	I	The signal will reset the CTP,Signal is active low
2	**CTP-VDD2.8V**	P	Power supply for CTP(2.8V)
3	**GND**	P	Power Ground
4	**CTP-INT(1.8V)**	I	Interrupt signals for CTP
5	**CTP-SDA(1.8V)**	I	I2C data signal for CTP
6	**CTP-SCL(1.8V)**	I	I2C clock signal for CTP

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	VDD	-	3.3	-	V	-
Power Supply2 Voltage	IOVCC	1.7	1.8	2.0	V	-
Power Supply4 Voltage	TP_VDD	2.7	2.8	3.4	V	-
Power Supply1 Current	I_{VDD}	-	TBD	-	mA	Note1
Power Supply4 Current	I_{TP_VDD}	-	TBD	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3IOVCC	V	-

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=3.3V,60Hz Refresh.

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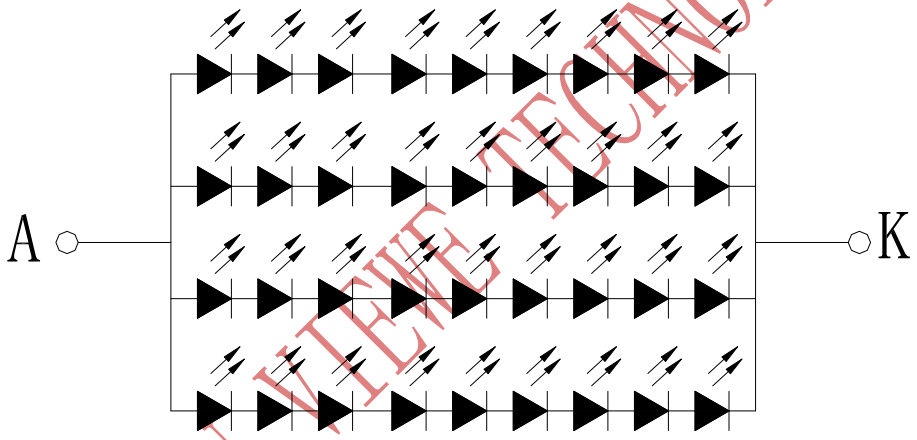
5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	25.2	27.0	28.8	V	Note1
Forward Current	I_F	-	92	-	mA	Note1
Backlight Power consumption	P_{BL}	-	2.484	-	Watt	Note1
LED life time	-	30000	-	-	Hrs	Note2
LED Quantity			36		PCS	

(Ta=+25°C,GND=0V)

Note1: The LED driving condition is defined for each LED module 。

Note2:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=23mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 23mA.



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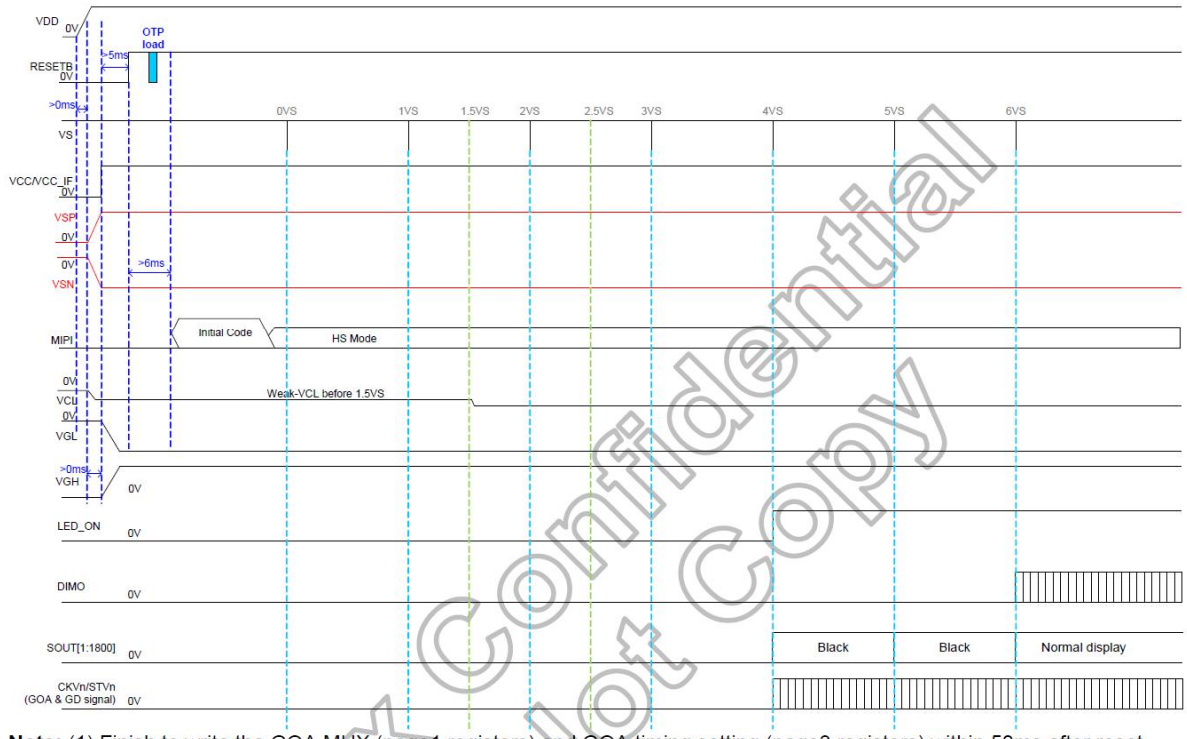
5.3 Power On/Off Sequence

LCM Power on:

After reset state or exit STB mode, the power on sequence will start. One SCHOTTKY diode is necessary between VGL and GND when VDD and VSP start at the same time.



Note: (1) Finish to write the GOA MUX (page1 registers) and GOA timing setting (page3 registers) within 50ms after reset pulls to high

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LCM Power off:

When enter STB mode, the STBYB signal will be set to low then the power off sequence will start.

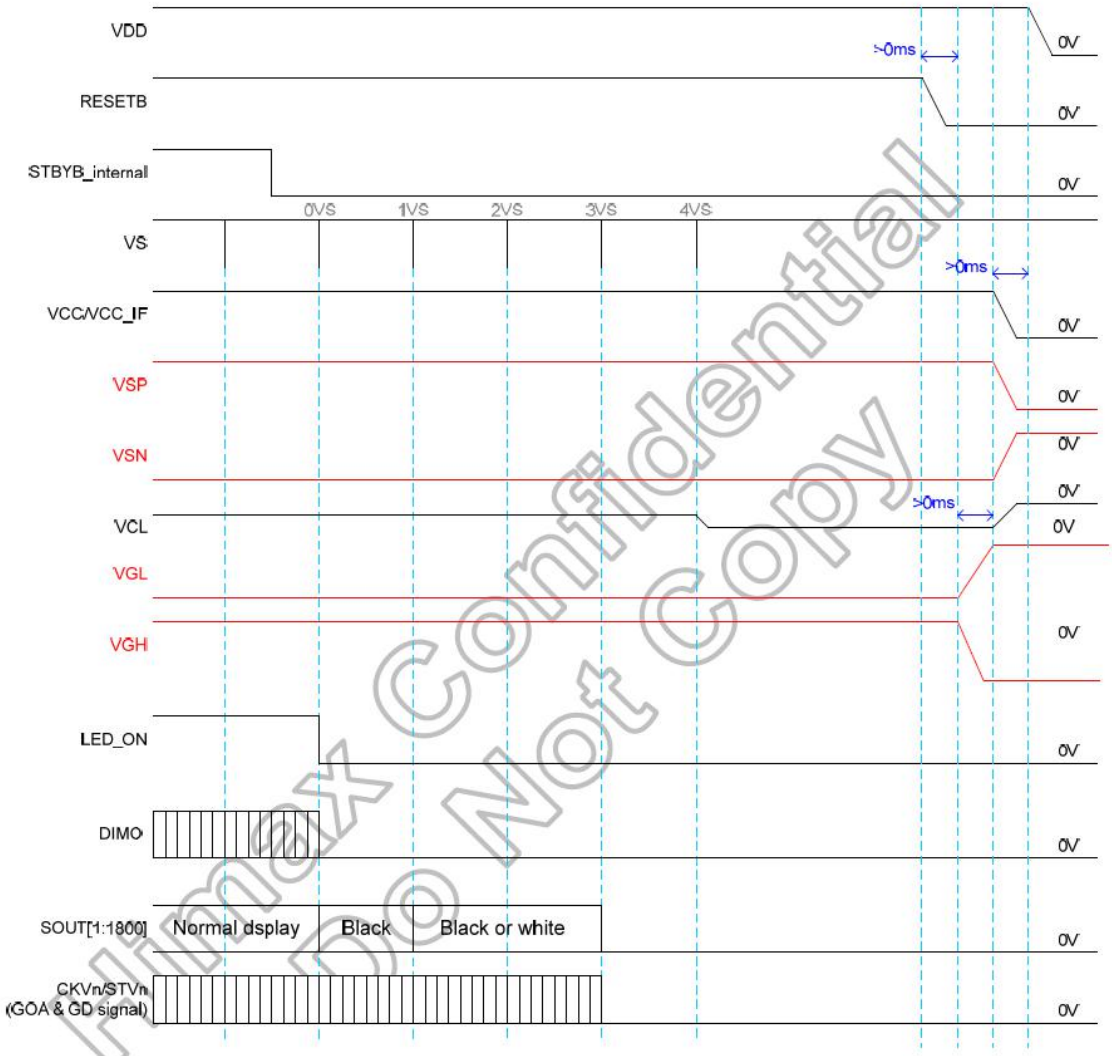

Figure 5.8: Power off sequence with PWRMD=1

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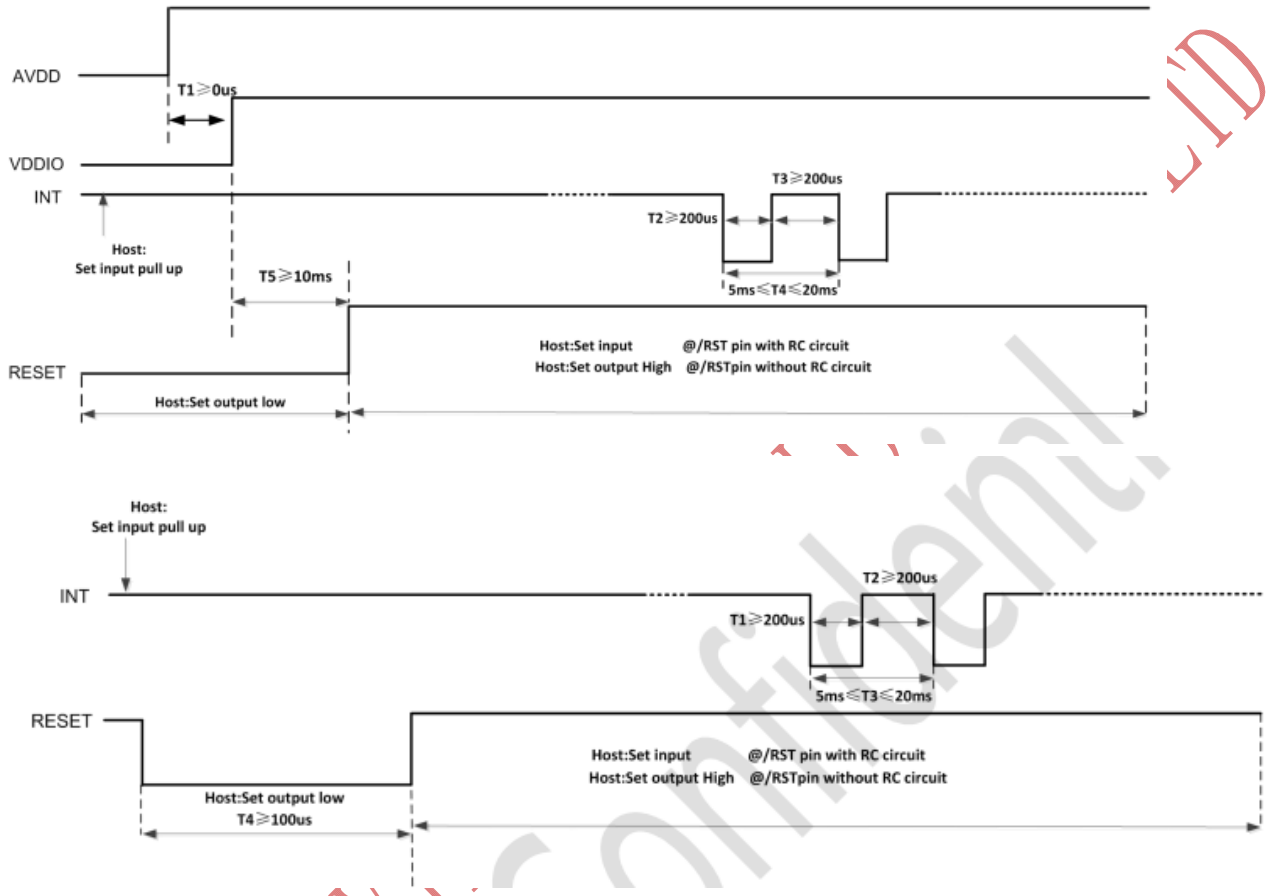
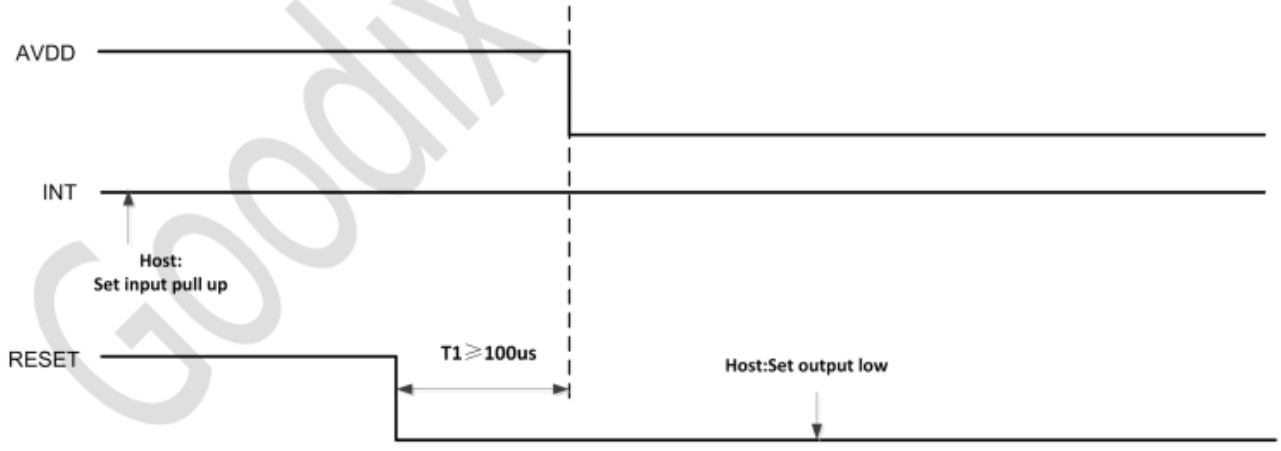
TP

上电时序图:



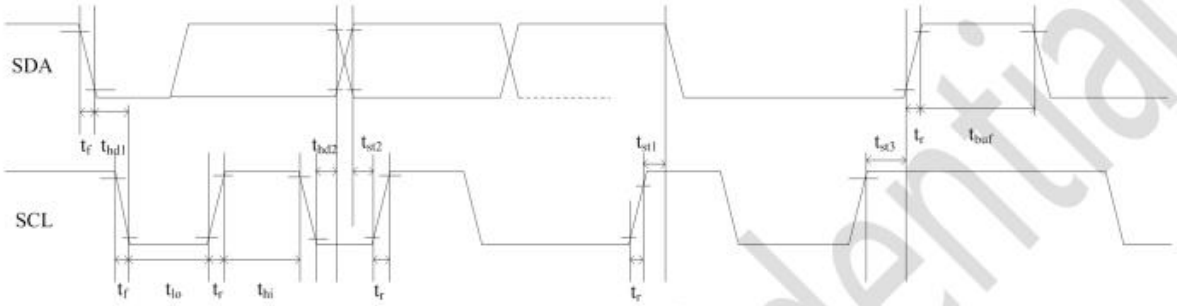
下电时序图:



5.4 AC Characteristics

5.4.1 TP AC Characteristics

通讯速度为 400Kbps 或以下。其支持的 I²C 硬件电路支持时序如下：



测试条件 2：3.3V 通讯接口，400Kbps 通讯速度，上拉电阻 2K

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

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5.4.2 LCM Characteristics

MIPI DC Characteristics:

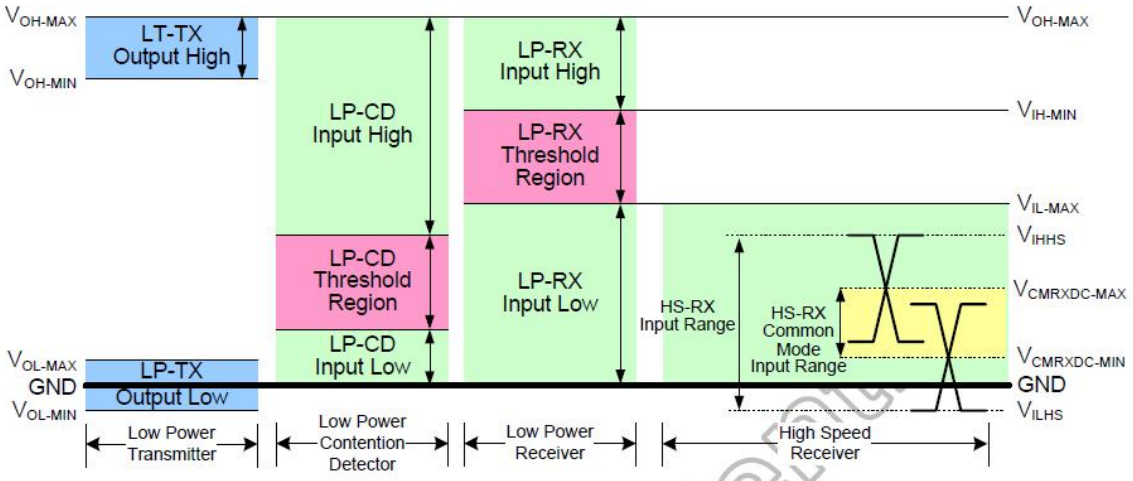

Figure 12.1: MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

DC characteristics for MIPI HS mode

Parameter	Symbol	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold(1)	V_{IDTH}	-	-	70	mV
Differential input low threshold(1)	V_{IDTL}	-70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage (VDP-VDN)	|VOD|	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

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MIPI AC Characteristics:

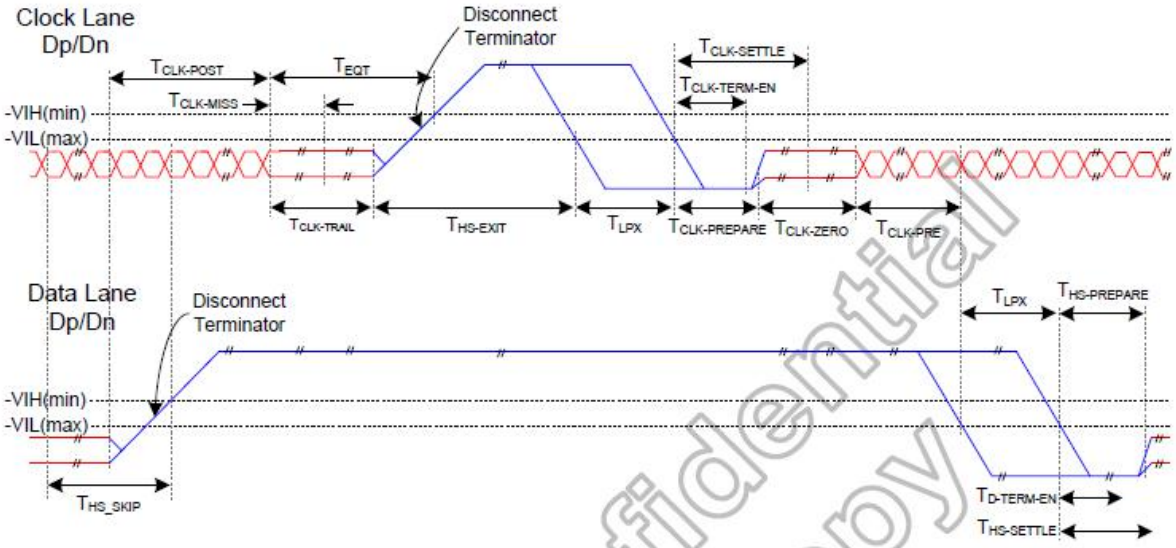


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

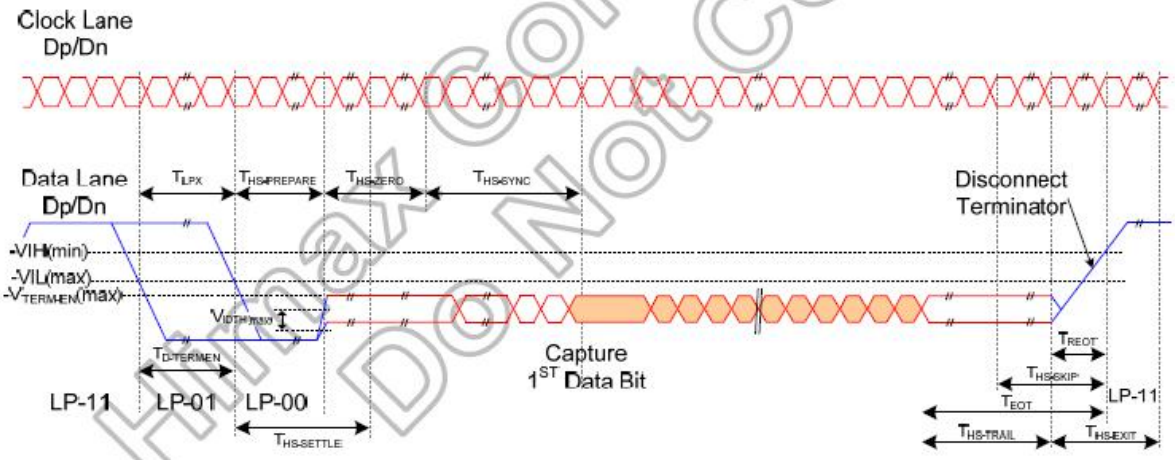
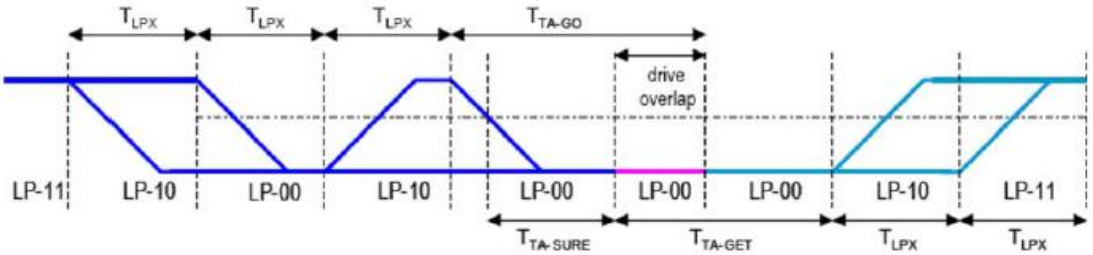


Figure 13.2: Timing of high-speed data transmission in bursts



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MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI (For DCS)	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$(1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}$/$T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX		5*T_{LPX}		ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request		4*T_{LPX}		ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	2*T_{LPX}	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

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5.5 Timing Diagram

MIPI data-clock timing :

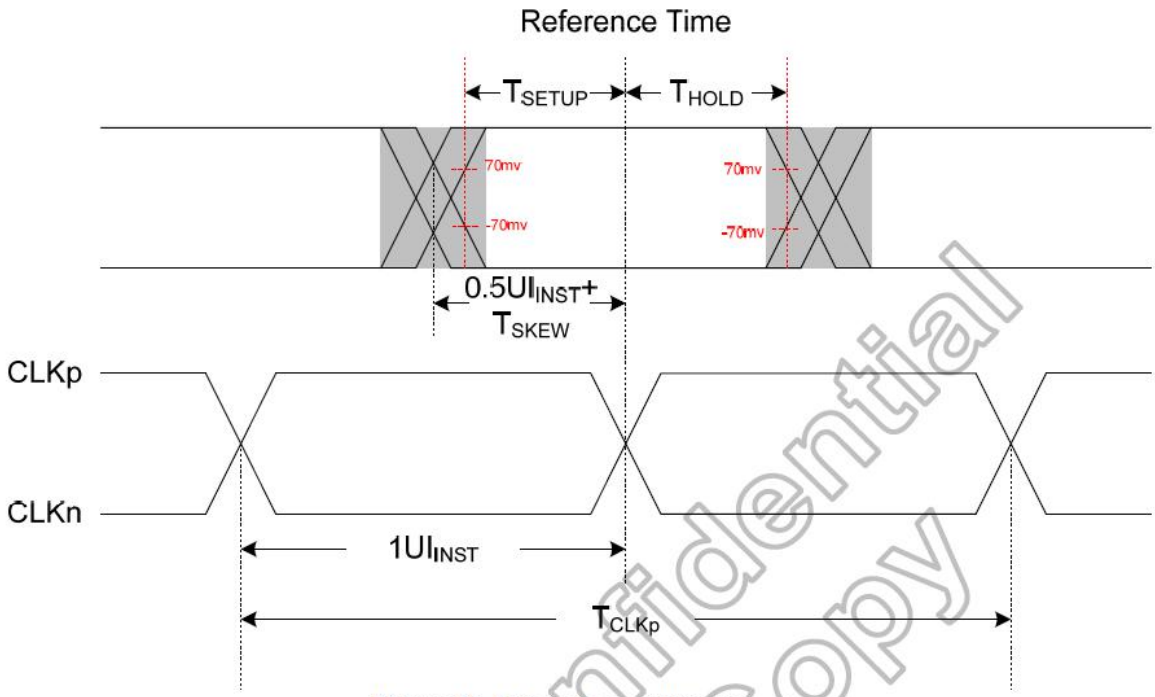

Figure 13.4: Data to clock timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
UI instantaneous	UI_{INST}	1.0	-	12.5(1)	ns
Data to clock setup time	T_{SETUP}	0.15	-	-	UI_{INST}
Data to clock hold time	T_{HOLD}	0.15	-	-	UI_{INST}

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

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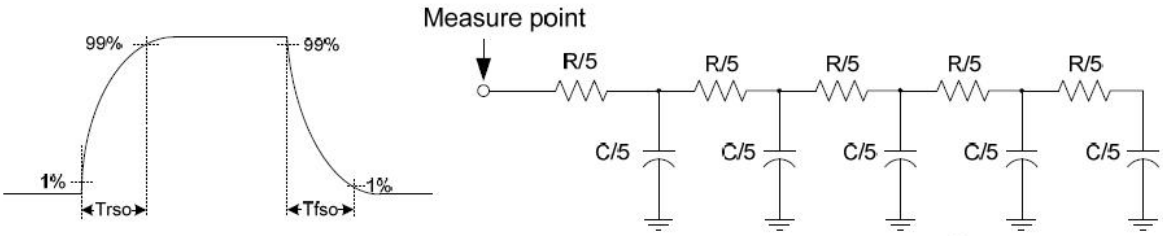
Source output timing:

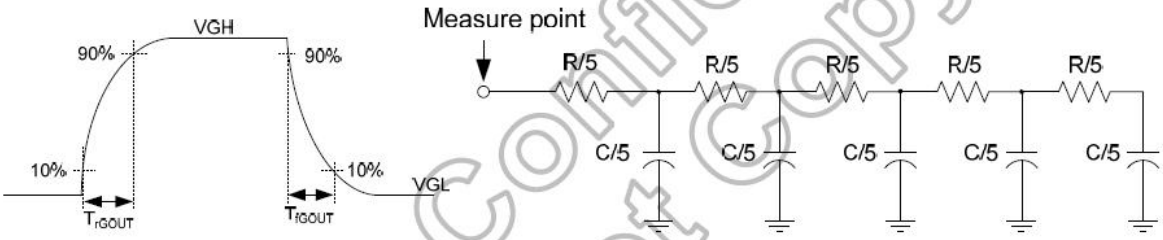


Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Source driver rising time	trSO	Load R=7.94KΩ, Load C = 85.84pF, Voltage: -5V←→5V VSN=-5.1V, VSP=5.1V	-	-	6.0	µs
Source driver falling time	tfSO		-	-	6.0	µs

Note: (1) Himax can support simulation for customer design.

Table 13.1: Source output timing

Panel control signal output 1 **(GOUT1_L~GOUT20_L, GOUT1_R~GOUT20_R)**



Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Panel control signal rising time	T_{rGOUT}	LOAD R=1780Ω LOAD C=1273pF VGH=+16V, VGL=-16.0V	-	-	5	µs
Panel control signal falling time	T_{fGOUT}		-	-	5	µs

Note: (1) Himax can support simulation for customer design.

Table 13.2: GOA output timing

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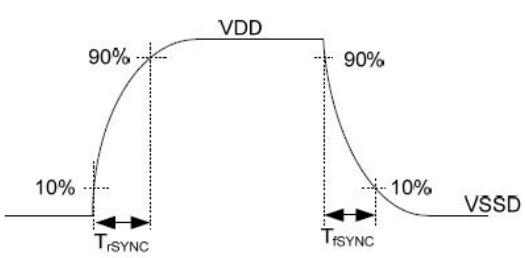
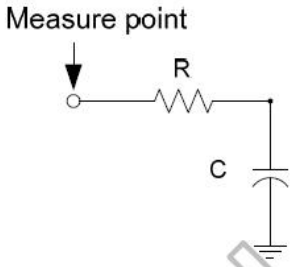
Panel control signal output 2 **(SYNC1_L~ SYNC8_L, SYNC1_R~ SYNC8_R)**





Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Panel synchronization signal rising time	T_{rSYNC}	LOAD R = 1KΩ	-	-	60	ns
Panel synchronization signal falling time	T_{fSYNC}	LOAD C = 40pF	-	-	60	ns

Note: (1) Himax can support simulation for customer design.

Table 13.3: Synchronization signals output timing

Timing requirements for reset:

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of low can be shown as the following.

(VDD=1.7V~2.0V, VSS=0V, T_{OPR} =-20℃~+85℃)

Parameter	Symbol	Conditions	Spec. Min.	Spec. Typ.	Spec. Max.	Unit
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.5: Reset timing

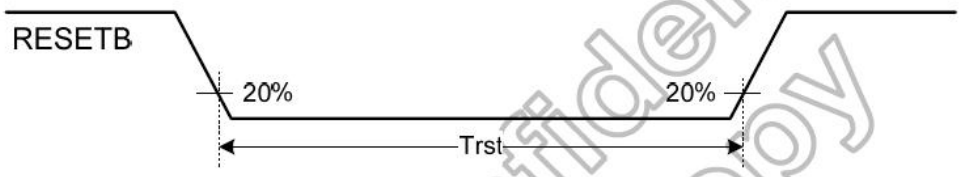


Figure 13.6: Reset timing

6 . Code

```
//HS=12 HBP=30 HFP=20
//VS=4 VBP=10 VFP=14
//FPS=60hz


init code:
Generic_Short_Write_1P(0xB0,0x00);  //PAGE0
Generic_Short_Write_1P(0xBD,0x44);//VCOM
Generic_Short_Write_1P(0xC2,0x08);    //0C
Generic_Short_Write_1P(0xC4,0x10);    //0C

Generic_Short_Write_1P(0xB0,0x02);  //PAGE2
Generic_Short_Write_1P(0xC0,0x00);
Generic_Short_Write_1P(0xC1,0x0A);
Generic_Short_Write_1P(0xC2,0x13);
Generic_Short_Write_1P(0xC3,0x20);
Generic_Short_Write_1P(0xC4,0x1F);
Generic_Short_Write_1P(0xC5,0x1E);
Generic_Short_Write_1P(0xC6,0x1D);
Generic_Short_Write_1P(0xC7,0x1C);
Generic_Short_Write_1P(0xC8,0x19);
Generic_Short_Write_1P(0xC9,0x17);
Generic_Short_Write_1P(0xCA,0x17);
Generic_Short_Write_1P(0xCB,0x18);
Generic_Short_Write_1P(0xCC,0x1A);
Generic_Short_Write_1P(0xCD,0x1E);
Generic_Short_Write_1P(0xCE,0x20);
Generic_Short_Write_1P(0xCF,0x23);
Generic_Short_Write_1P(0xD0,0x07);
Generic_Short_Write_1P(0xD1,0x00);
Generic_Short_Write_1P(0xD2,0x00);
Generic_Short_Write_1P(0xD3,0x0A);
Generic_Short_Write_1P(0xD4,0x13);
Generic_Short_Write_1P(0xD5,0x20);
Generic_Short_Write_1P(0xD6,0x1F);
Generic_Short_Write_1P(0xD7,0x1E);
Generic_Short_Write_1P(0xD8,0x1D);
Generic_Short_Write_1P(0xD9,0x1C);
Generic_Short_Write_1P(0xDA,0x19);
Generic_Short_Write_1P(0xDB,0x17);
Generic_Short_Write_1P(0xDC,0x17);
Generic_Short_Write_1P(0xDD,0x18);
Generic_Short_Write_1P(0xDE,0x1A);
Generic_Short_Write_1P(0xDF,0x1E);
Generic_Short_Write_1P(0xE0,0x20);
Generic_Short_Write_1P(0xE1,0x23);
Generic_Short_Write_1P(0xE2,0x07);

//////////////////////////////////////////
Generic_Short_Write_1P(0xB0,0x01);
Generic_Short_Write_1P(0xC3,0x0F);
Generic_Short_Write_1P(0xC4,0x00);
```

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```
Generic_Short_Write_1P(0xC5,0x00);
Generic_Short_Write_1P(0xC6,0x00);
Generic_Short_Write_1P(0xC7,0x00);
Generic_Short_Write_1P(0xC8,0x0D);
Generic_Short_Write_1P(0xC9,0x12);
Generic_Short_Write_1P(0xCA,0x11);
Generic_Short_Write_1P(0xCD,0x1D);
Generic_Short_Write_1P(0xCE,0x1B);
Generic_Short_Write_1P(0xCF,0x0B);
Generic_Short_Write_1P(0xD0,0x09);
Generic_Short_Write_1P(0xD1,0x07);
Generic_Short_Write_1P(0xD2,0x05);
Generic_Short_Write_1P(0xD3,0x01);
Generic_Short_Write_1P(0xD7,0x10);
Generic_Short_Write_1P(0xD8,0x00);
Generic_Short_Write_1P(0xD9,0x00);
Generic_Short_Write_1P(0xDA,0x00);
Generic_Short_Write_1P(0xDB,0x00);
Generic_Short_Write_1P(0xDC,0x0E);
Generic_Short_Write_1P(0xDD,0x12);
Generic_Short_Write_1P(0xDE,0x11);
Generic_Short_Write_1P(0xE1,0x1E);
Generic_Short_Write_1P(0xE2,0x1C);
Generic_Short_Write_1P(0xE3,0x0C);
Generic_Short_Write_1P(0xE4,0x0A);
Generic_Short_Write_1P(0xE5,0x08);
Generic_Short_Write_1P(0xE6,0x06);
Generic_Short_Write_1P(0xE7,0x02);

//PAGE3
Generic_Short_Write_1P(0xB0,0x03);
Generic_Short_Write_1P(0xBE,0x03);
Generic_Short_Write_1P(0xCC,0x44);
Generic_Short_Write_1P(0xC8,0x07);
Generic_Short_Write_1P(0xC9,0x05);
Generic_Short_Write_1P(0xCA,0x42);
Generic_Short_Write_1P(0xCD,0x3E);
Generic_Short_Write_1P(0xCF,0x60);
Generic_Short_Write_1P(0xD2,0x04);
Generic_Short_Write_1P(0xD3,0x04);
Generic_Short_Write_1P(0xD4,0x01);
Generic_Short_Write_1P(0xD5,0x00);
Generic_Short_Write_1P(0xD6,0x03);
Generic_Short_Write_1P(0xD7,0x04);
Generic_Short_Write_1P(0xD9,0x01);
Generic_Short_Write_1P(0xDB,0x01);
Generic_Short_Write_1P(0xE4,0xF0);
Generic_Short_Write_1P(0xE5,0x0A);


//Generic_Short_Write_1P(0xB0,0x05);      //PAGE5
//Generic_Short_Write_1P(0xC0,0x01);
//Generic_Short_Write_1P(0xC2,0x01);
//Generic_Short_Write_1P(0xD9,0x01);
```

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```
//Generic_Short_Write_1P(0xDB,0x01);

    DCS_Short_Write_NP(0x11);
    Delay(800);
    DCS_Short_Write_NP(0x29);
    Delay(20);
```

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7. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	□= 0□	800	1000	-	-	Note(4)
NTSC Ratio	S	□=0□	-	65	-	%	Note(7)
Luminance	L	□=0□	350	400	-	cd/m2	Note(5)
Luminance uniformity	Uw	□=0□	-	80	-	□	Note(3)
Response Time	TR+ TF	25 □C	-	25	-	ms	Note(2)
Color Coordination	Wx	□= 0□ (Center) Normal viewing angle B/L On	-0.04	0.305	+0.04	NTSC (x,y)	Note(6)
	Wy			0.320			
	Rx			0.651			
	Ry			0.331			
	Gx			0.275			
	Gy			0.56			
	Bx			0.140			
	By			0.095			
Viewing Angle	θ L	C/R□10	80	85	-	Degree	Note(1)
	θ R		80	85	-		
	θ U		80	85	-		
	θ D		80	85	-		

Test Conditions:

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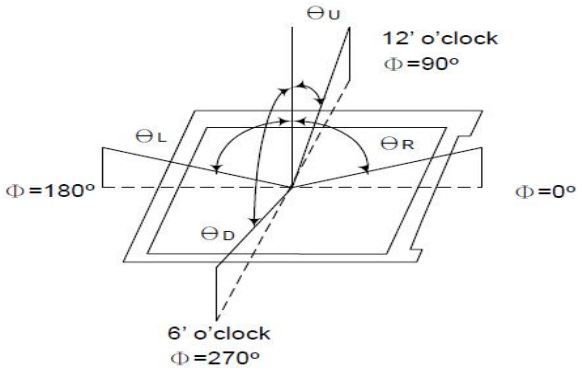
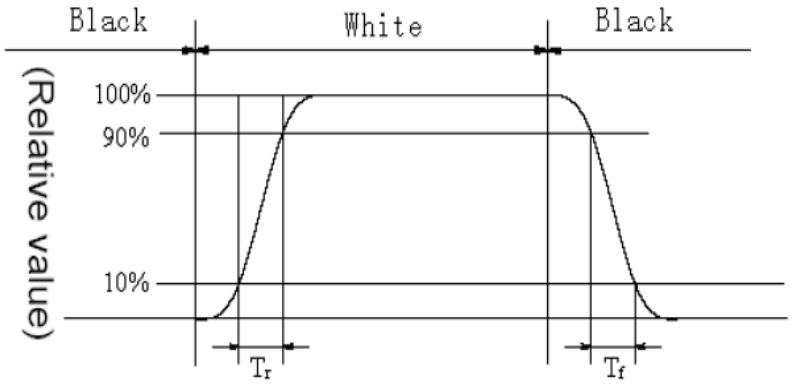
1. IOVCC=1.8V, I_F=92mA (Backlight current), the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR□10

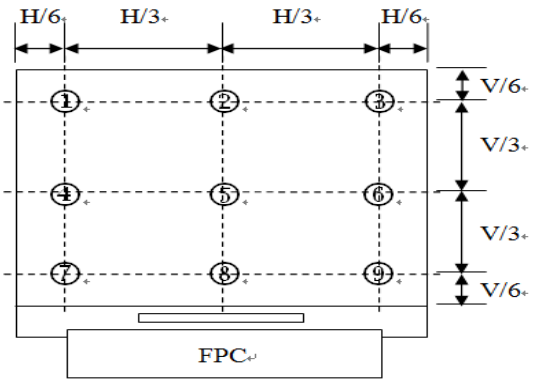


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \text{ x100\%}$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

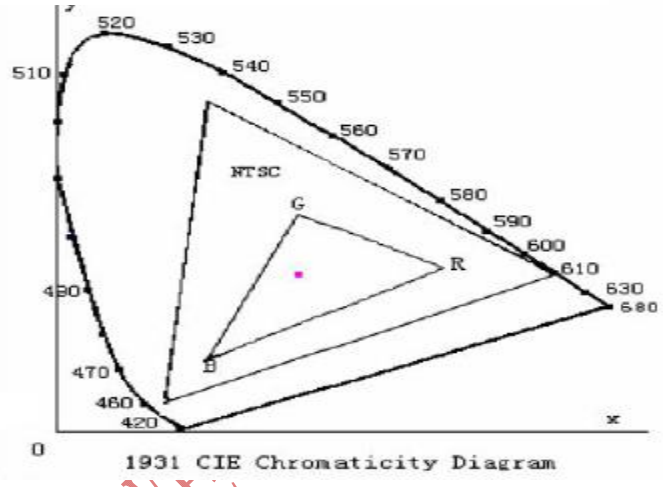
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

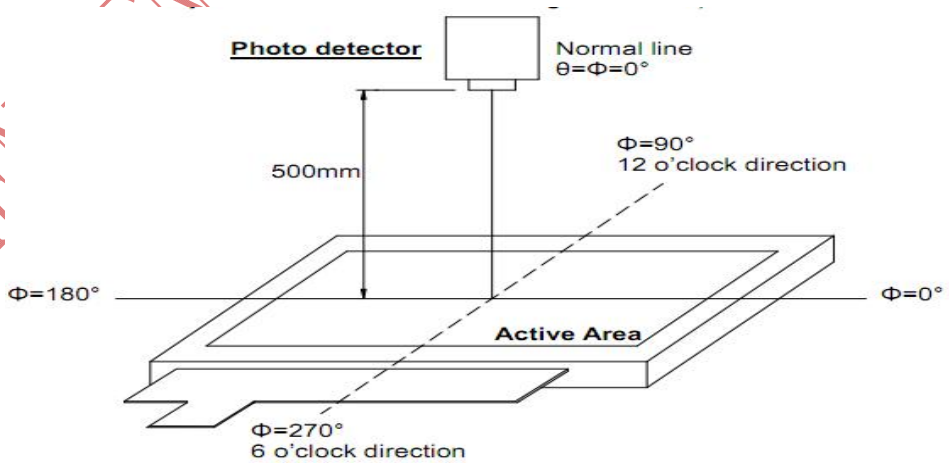
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



8. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+60°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-20°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+50°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-10°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-20°C/30min □+60°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 60cm height, 1 corner, 3 edges, 6 surfaces.	Note2

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

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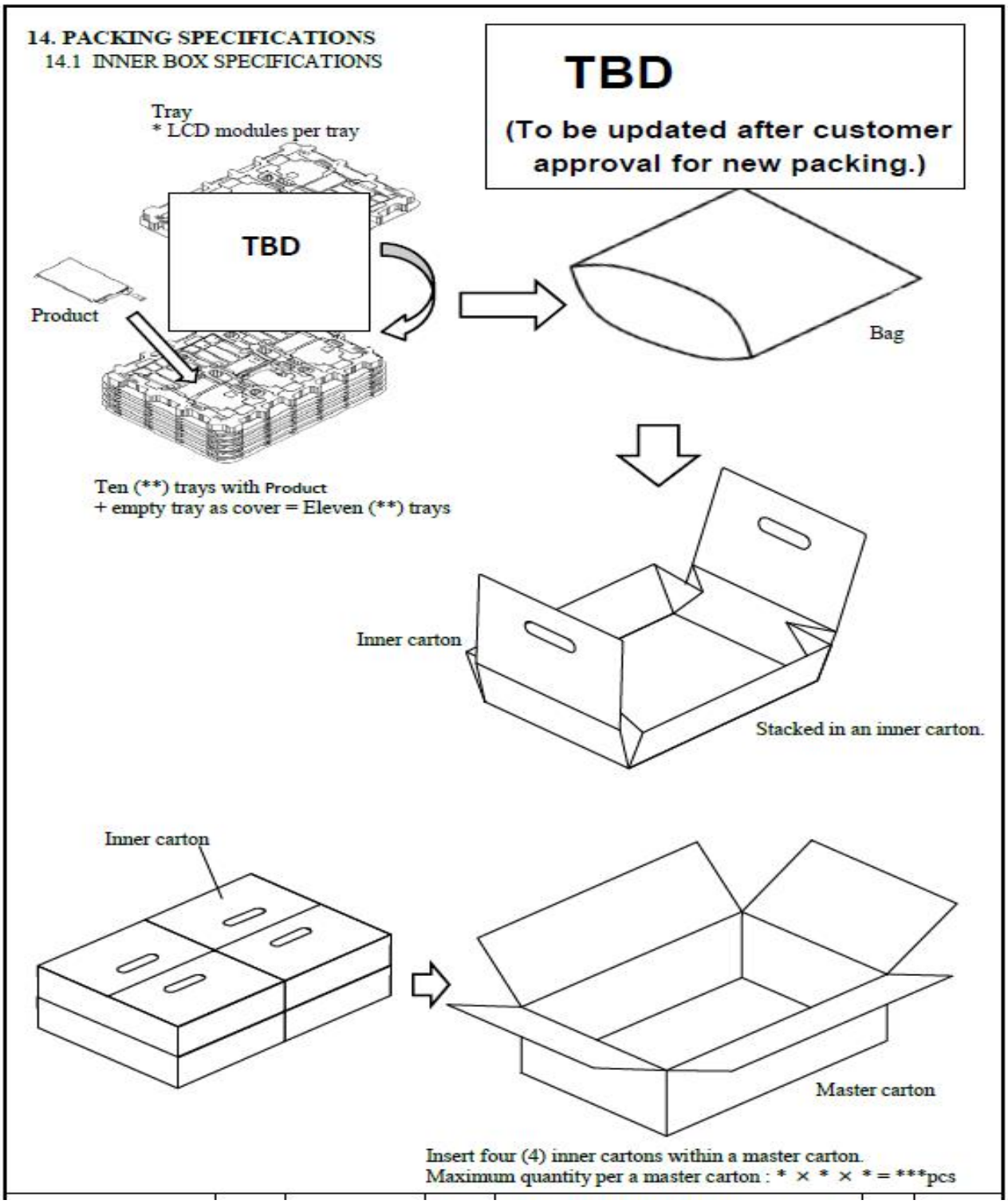
9. PACKAGE DRAWING