LCD MODULE

SPECIFICATION

Model:	UE055HD-AP40-A047D
Version:	V1.3
Date:	20211125

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Customer Confirmation 客户确认

Approved by	Notes

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Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20210304	Preliminary release	
V1.1	20210517	Modify driver IC, LCD FPC shape, LCD id0 connection element area and conductive adhesive thickness	
V1.2	20210727	Modify TP / LCD FPC, TPVA and sensor, increase the number of channels, and adjust the IR hole design	
V1.3	20211125	Modify TP appearance size / sensor size / add black Mylar tape	

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1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode： MIPI
3) Driver IC： ILI9881P；Touch IC：GT1151Q
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode：Normally Black
8) Pixel Density：295 PPI
9) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	5.45	Inch	Diagonal
Resolution	720(W)*3(RGB)*1440(H)	Dots	-
Interface	MIPI	-	4 lanes
Module Power Consumption	1.046	Watt	Typ.
Active Area	61.88(W)*123.77(H)	mm	-
Pixel pitch (W*H)	0.02865(W)*0.08595(H)	mm	-
CTP_Module Size (W*H*D)	69.2(W)*154.3(H)*2.85(D)	mm	Typ
Luminance	500	cd/m^2	Typ.
Viewing Direction	ALL	O'clock	
Display Color	16.7M	Colors	24bits

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2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	IOVCC	-0.3	3.8	V	Note1
Power supply2 voltage	VSP	-0.3	7.0	V	Note1
Power supply3 voltage	VSN	-7.0	0.3	V	Note1
LED forward current	I_F	-0.001	20	mA	For each led,Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1
Operating temperature	T_{op}	-20	70	℃	Note1,2
Storage temperature	T_{st}	-30	80	℃	Note1,2
Humidity	H_{st}	10	90	%RH	Note1,3

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

Note2: In case of temperature below 0℃,the response time of liquid crystal (LC) becomes slower and the color of panel darker than normal one.

Note3: Temp. ≤ 60℃ , 90% RH MAX.

Temp. ＞60℃ , Absolute humidity shall be less than 90% RH at 60℃.

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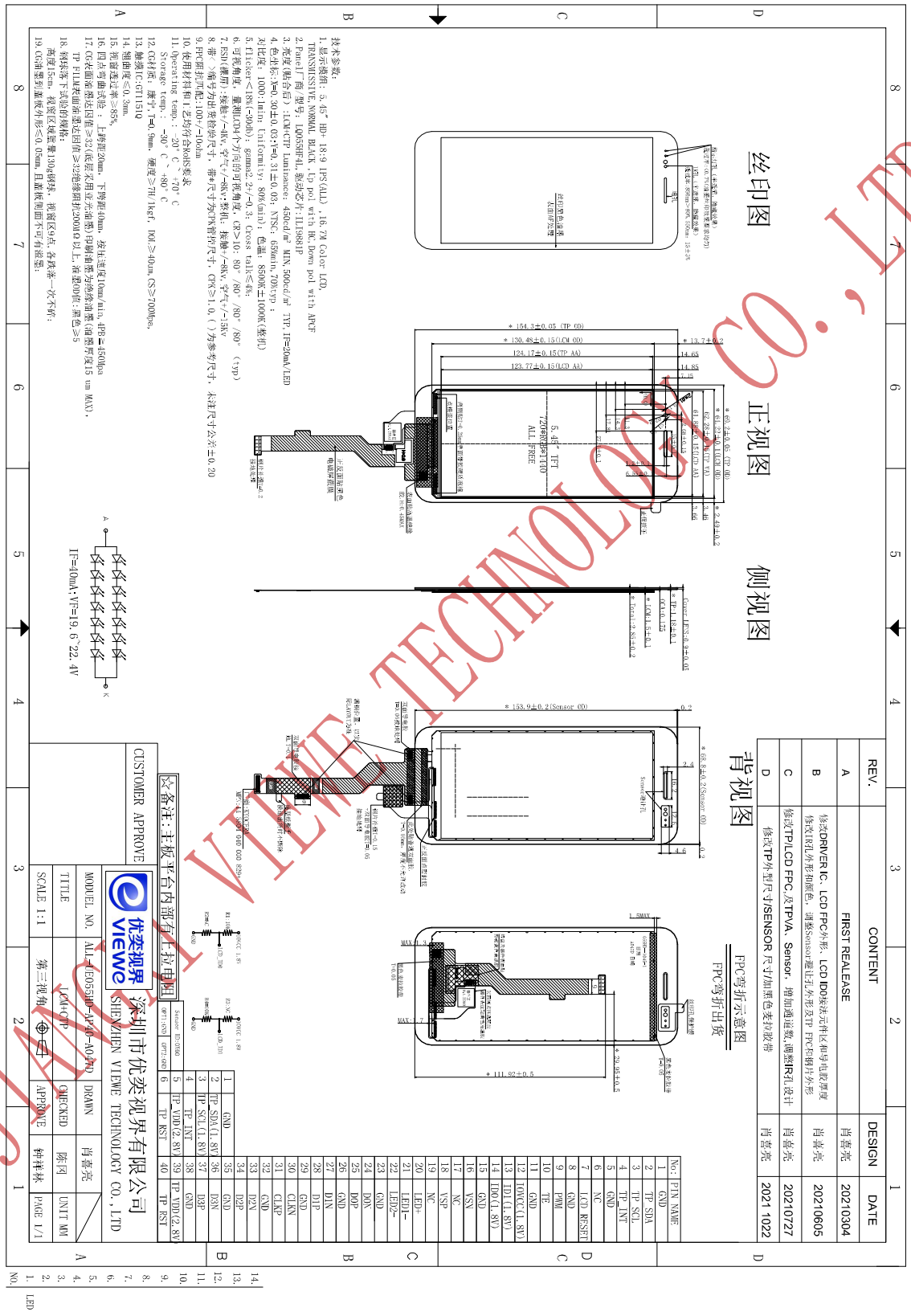
3. MECHANICAL DRAWING



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4. I/O CONNECTION & BLOCK DIAGRAM

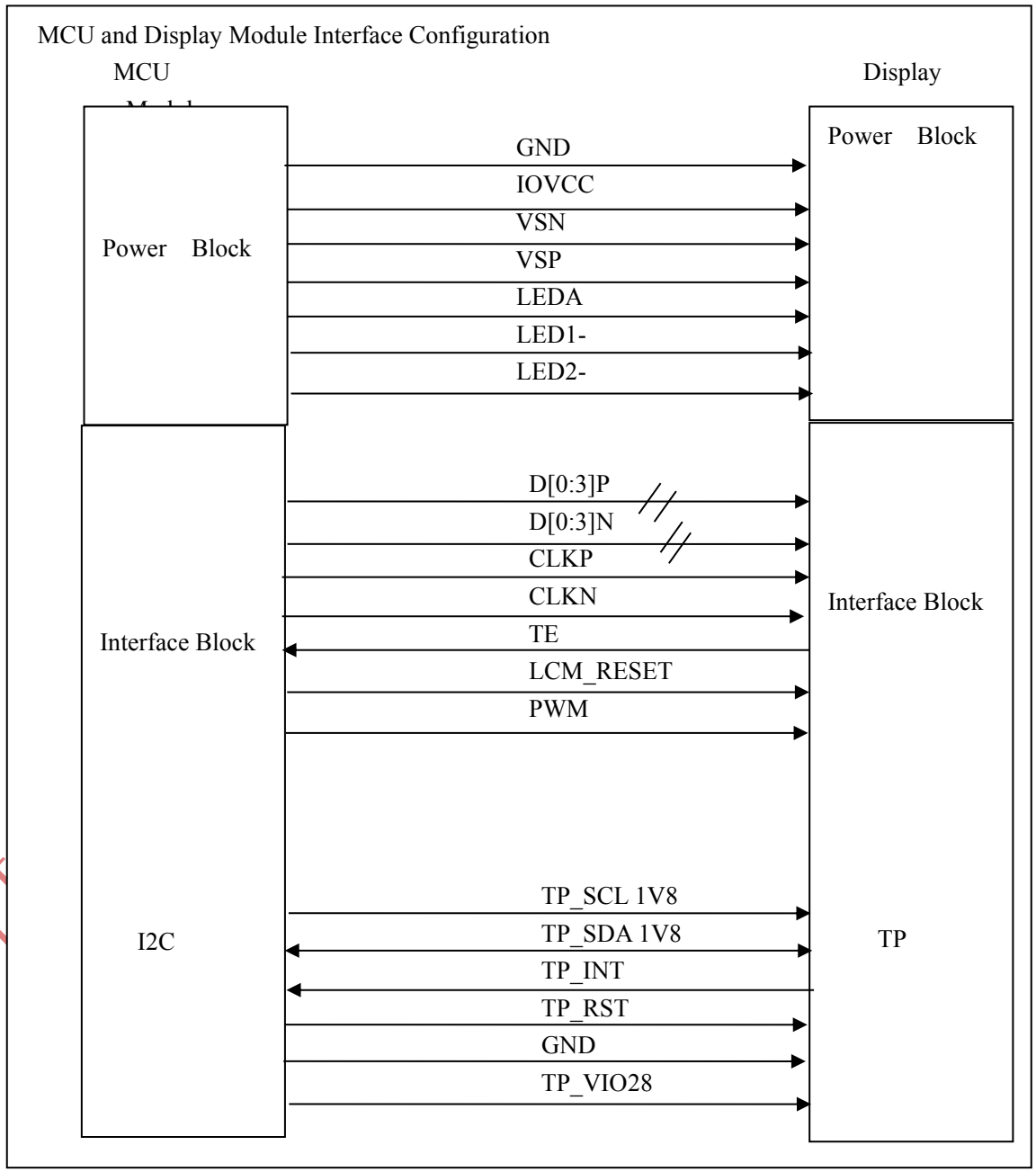
4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**GND**	P	Power Ground
2	**TP_SDA**	I/O	I2C data signal for TP
3	**TP_SCL**	I	I2C data signal for TP
4	**TP_INT**	O	Interrupt signals for TP
5	**GND**	P	Power Ground
6	**NC**	-	No connected
7	**LCD_RESET**	I	The signal will reset the LCM, Signal is active low.
8	**GND**	P	Power Ground
9	**PWM**	I	This pin is connecting with the external LED driver
10	**TE**	O	Tearing effect outputsignal. If not used, please let this pin
11	**GND**	P	Power Ground
12	**IOVCC(1.8V)**	P	Power supply to interface pins(1.8V)
13	**ID1(1.8V)**	O	LCD ID0
14	**ID0(1.8V)**	O	LCD ID0
15	**GND**	P	Power Ground
16	**VSN**	P	Negative input analog power for driver IC use
17	**NC**	-	No connected
18	**VSP**	P	Positive input analog power for driver IC use
19	**NC**	-	No connected
20	**LED+**	P	Power supply for backlight anode
21	**LED1-**	P	Power supply for backlight cathode
22	**LED2-**	P	Power supply for backlight cathode
23	**GND**	P	Power Ground
24	**D0N**	I/O	MIPI-DSI data lane 0 negative-end input pin
25	**D0P**	I/O	MIPI-DSI data lane 0 positive-end input pin
26	**GND**	P	Power Ground
27	**D1N**	I	MIPI-DSI data lane 1 negative-end input pin
28	**D1P**	I	MIPI-DSI data lane 1 positive-end input pin
29	**GND**	P	Power Ground
30	**CLKN**	I	MIPI-DSI clock lane negative-end input pin
31	**CLKP**	I	MIPI-DSI clock lane positive-end input pin
32	**GND**	P	Power Ground
33	**D2N**	I	MIPI-DSI data lane 2 negative-end input pin
34	**D2P**	I	MIPI-DSI data lane 2 positive-end input pin
35	**GND**	P	Power Ground
36	**D3N**	I	MIPI-DSI data lane 3 negative-end input pin
37	**D3P**	I	MIPI-DSI data lane 3 positive-end input pin
38	**GND**	P	Power Ground
39	**TP_VDD(2.8V)**	P	Power supply for TP
40	**TP_RST**	I	The signal will reset the TP,Signal is active low

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**GND**	P	Power Ground
2	**TP_SDA(1.8V)**	I/O	I2C data signal for TP
3	**TP_SCL(1.8V)**	I	I2C data signal for TP
4	**TP_INT**	O	Interrupt signals for TP
5	**TP_VDD(2.8V)**	P	Power supply for TP
6	**TP_RST**	I	The signal will reset the TP,Signal is active low

I：Input；O：Output；P：Power

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.65	1.8	3.6	V	-
Power Supply2 Voltage	VSN	-6.2	-5.5	-4.5	V	-
Power Supply3 Voltage	VSP	4.5	5.5	6.2	V	-
Power Supply1 Current	I_{IOVCC}		20		mA	Note1
Power Supply2 Current	I_{VSN}		10		mA	Note1
Power Supply3 Current	I_{VSP}		10		mA	Note1
Logic Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3IOVCC	V	-
Panel Power Consumption	P_{VDD}	-	0.15	-	Watt	Note1
Module Power Consumption	P_{LCM}	-	1.046	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=1.8V,60Hz Refresh.

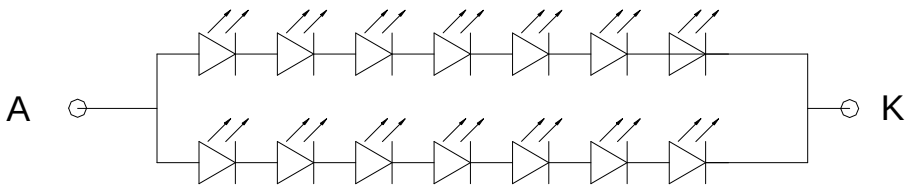
Note2: P_{LCM}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	19.6	-	22.4	V	Note1
Forward Current	I_F	-	40	-	mA	Note1
Backlight Power consumption	P_{BL}	0.784	-	0.896	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			14		PCS	

(Ta=+25°C,GND=0V)

Note1:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.



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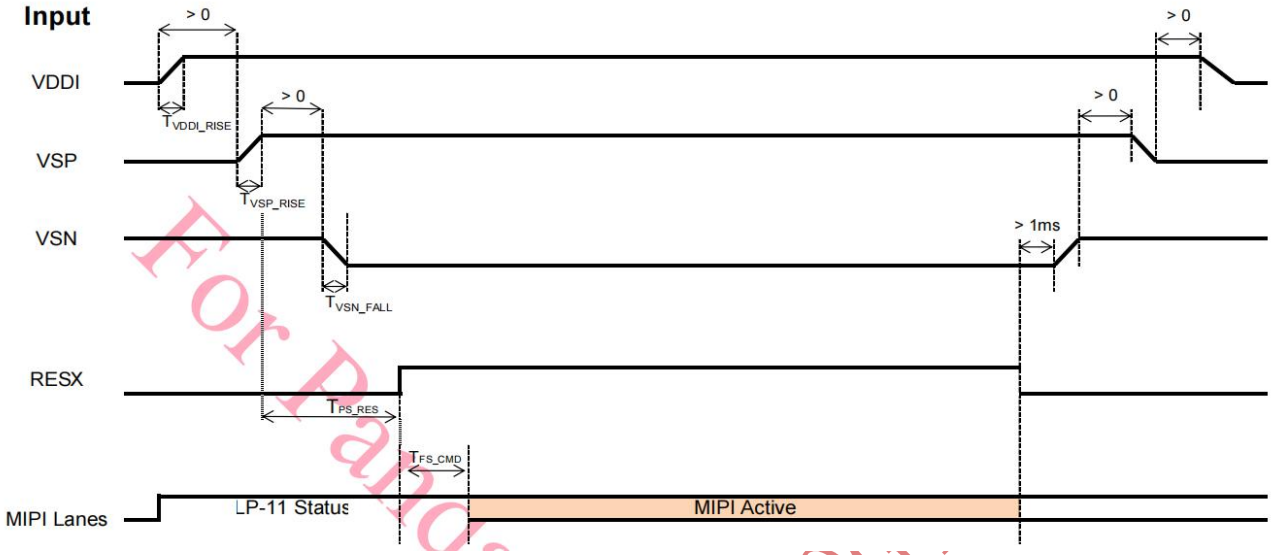
5.3 Power On/Off Sequence



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{FS_CMD}	Reset to first command	10	-	-	ms

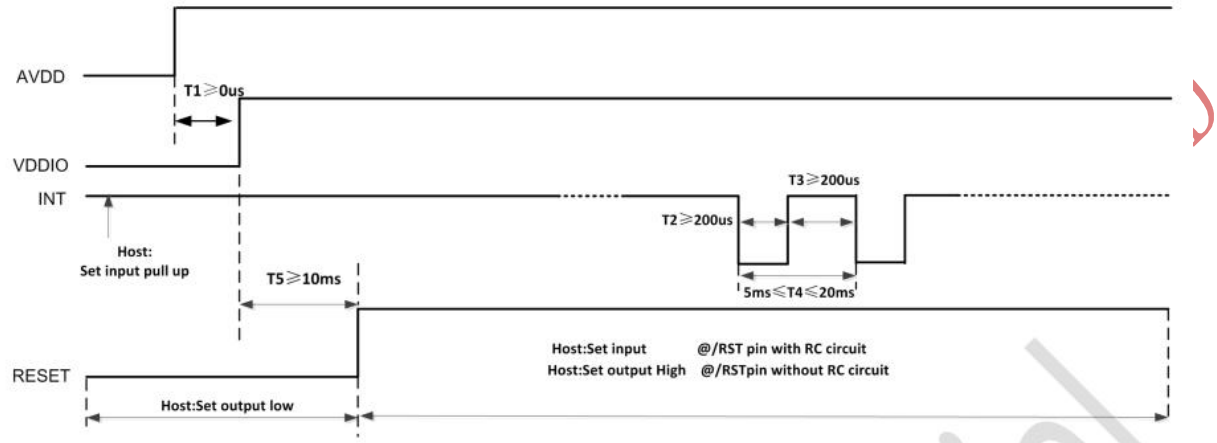
Figure 87: Power on/off sequence with 3 Power Mode

Uncontrolled Power Off

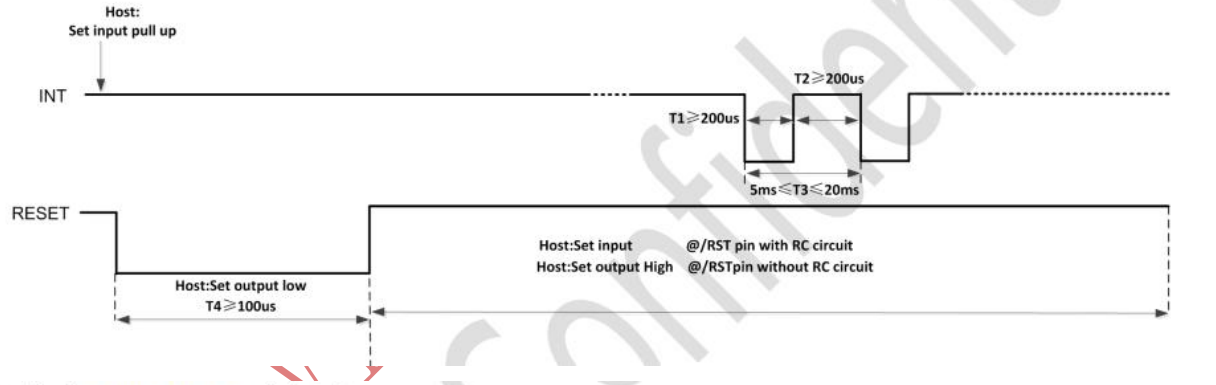
The uncontrolled power off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages for the display module, or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, the ILI9881P will force the display to become blank and will not have any abnormal visible effects within 1 second on the display and remains blank until the Power On Sequence powers it up.

For Panel reference only

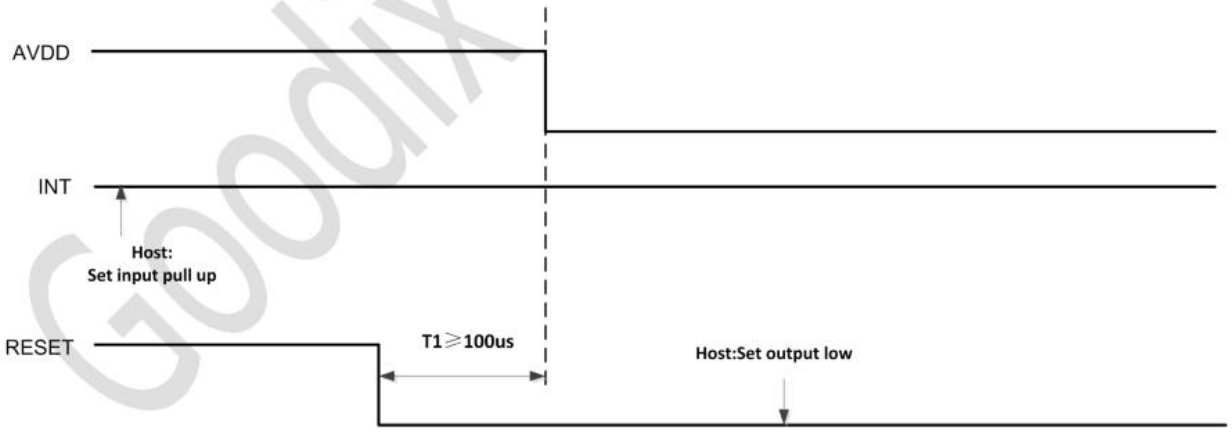
TP



主控复位 GT1151Q 时序图：



主控掉电 GT1151Q 时序图



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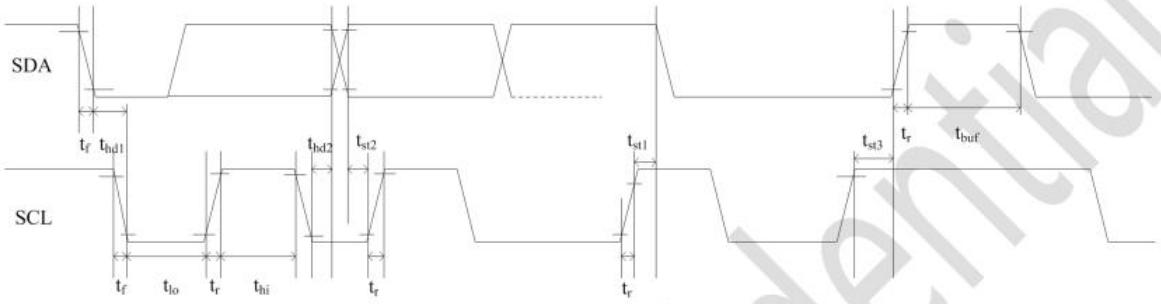
5.4 I2C interface timings

GT1151Q 提供标准的 I²C 通讯接口，由 SCL 和 SDA 与主 CPU 进行通讯。 在系统中 GT1151Q 始终作为从设备，地址为 0X28/0X29。所有通讯都是由主 CPU 发起，建议通讯速度为 400Kbps 或以下。其支持的 I²C 硬件电路支持时序如下：



测试条件 1：1.8V 通讯接口，400Kbps 通讯速度，上拉电阻 2K

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

测试条件 2：3.3V 通讯接口，400Kbps 通讯速度，上拉电阻 2K

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for START condition	t_{st1}	0.6	-	us
SCL setup time for STOP condition	t_{st3}	0.6	-	us
SCL hold time for START condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

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5.4.1 AC Characteristics

High Speed Mode – Clock Channel Timing

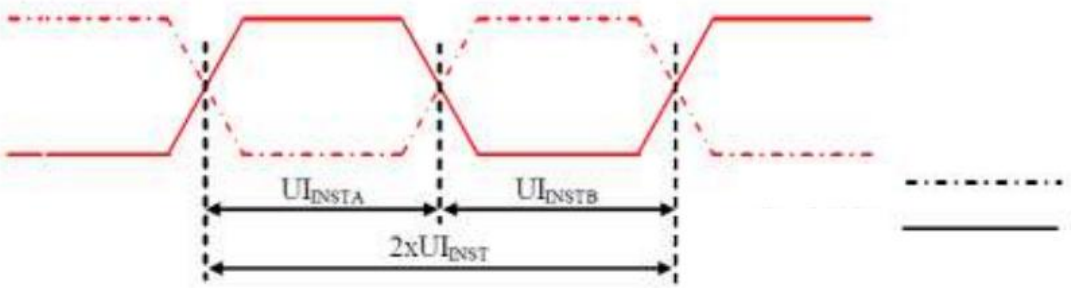

Figure 97: DSI Clock Channel Timing

Table 37: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 38.

Table 38: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850bps	700 Mbps	550 Mbps

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High Speed Mode – Data Clock Channel Timing

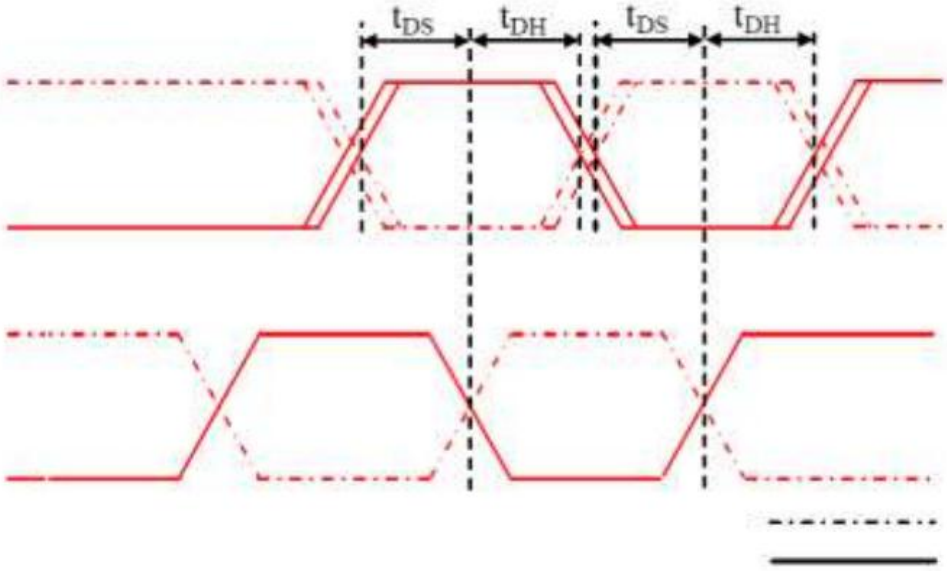

Figure 98: DSI Data to Clock Channel Timings

Table 39: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0,1,2,3	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

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High Speed Mode – Rising and Falling Timings

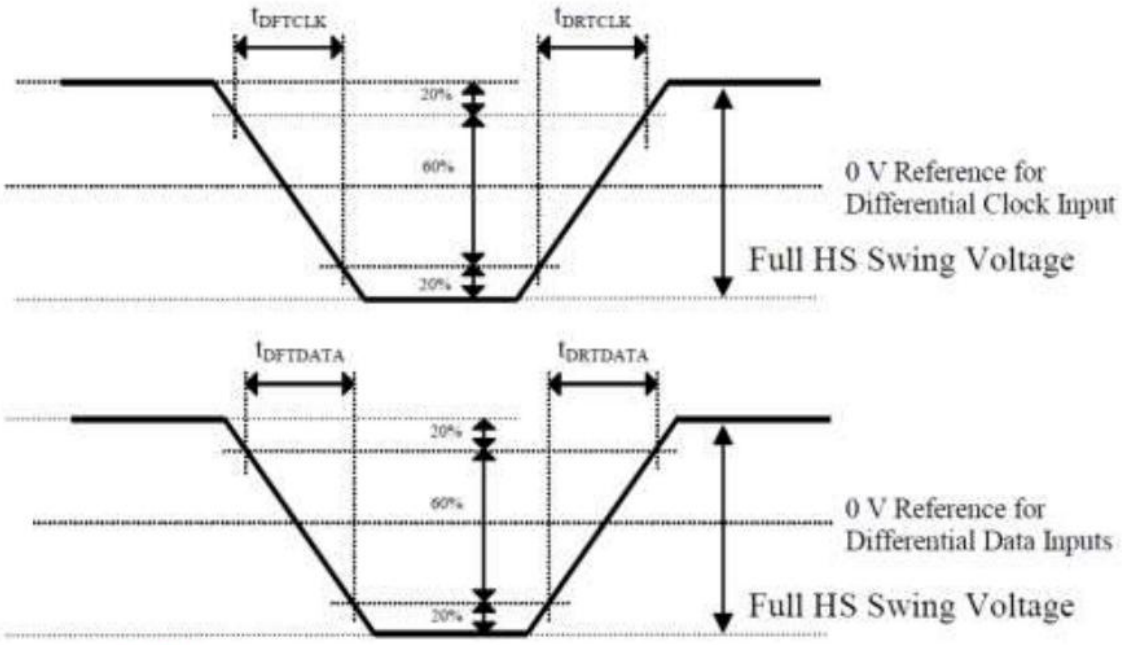

Figure 99: Rising and Falling Timings on Clock and Data Channels

Table 40: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0,1,2,3	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

Low Speed Mode - Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881P) are illustrated for reference purposes below.

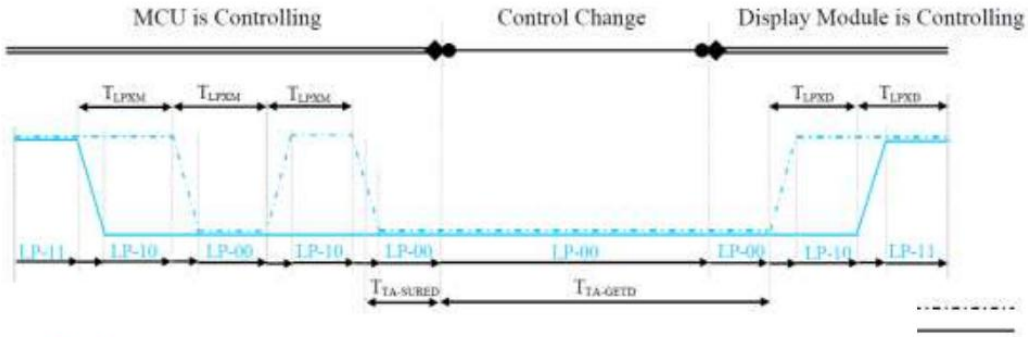

Figure 100: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881P) to the MCU are illustrated for reference purposes below.

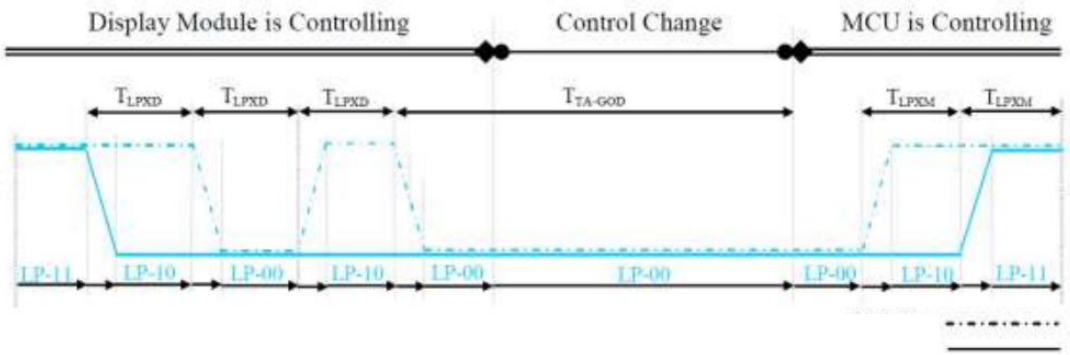

Figure 101: BTA from the Display Module to the MCU

Table 41: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881P)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881P) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881P) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 42: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881P)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4xT_{LPXD}$	ns

Data Lanes from Low Power Mode to High Speed Mode

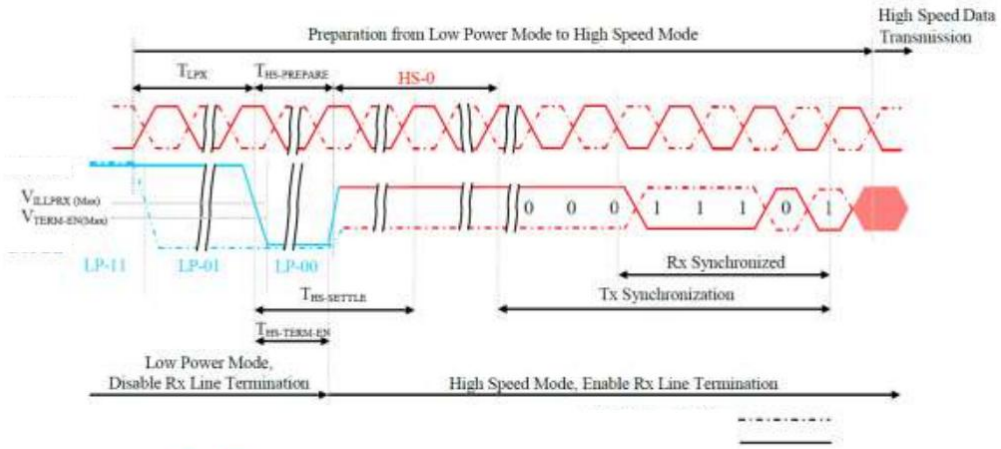

Figure 102: Data Lanes – Low Power Mode to High Speed Mode Timings

Table 43: Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0,1,2,3	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n=0,1,2,3	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n=0,1,2,3	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Data Lanes from High Speed Mode to Low Power Mode

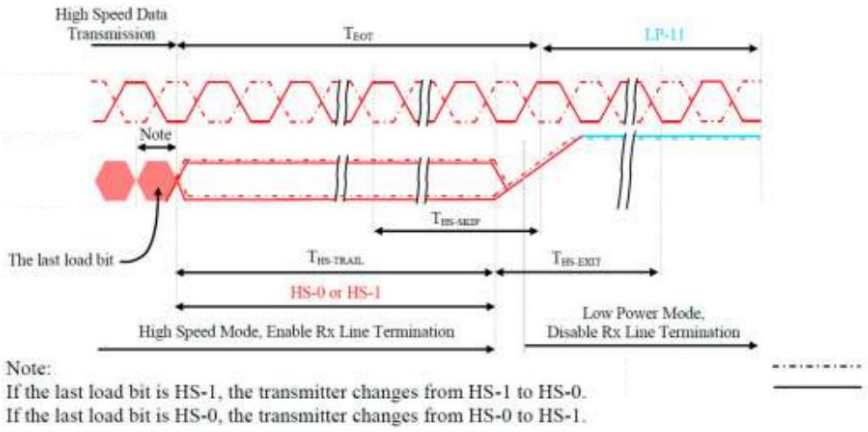

Figure 103: Data Lanes – High Speed Mode to Low Power Mode Timings

Table 44: Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n=0,1,2,3	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881P) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n=0,1,2,3	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DnP/N, n = 0,1,2,3	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	Max(8*UI,60ns+4*UI)	-	ns

DSI Clock Burst - High Speed Mode to/from Low Power Mode

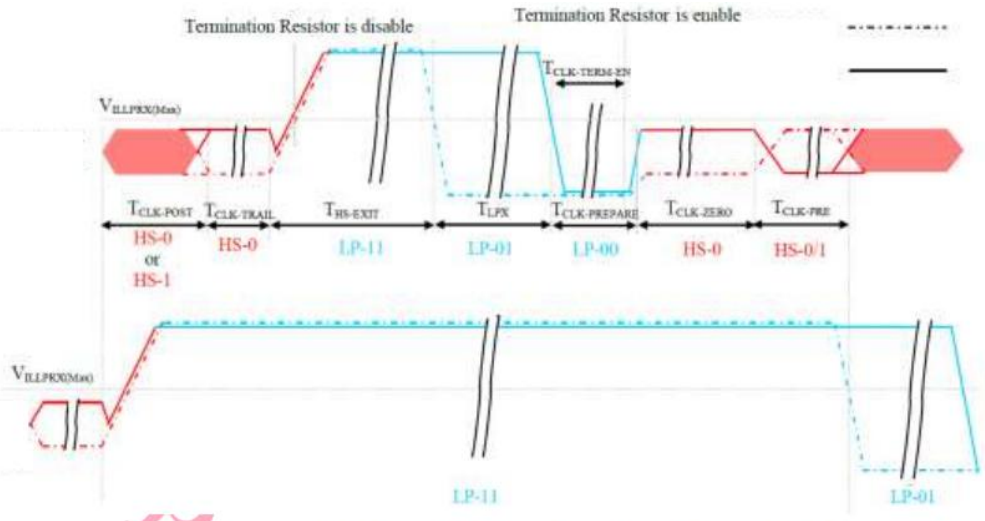

Figure 104: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 45: Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

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5.5 Timing Diagram

5.5.1 Reset Timing

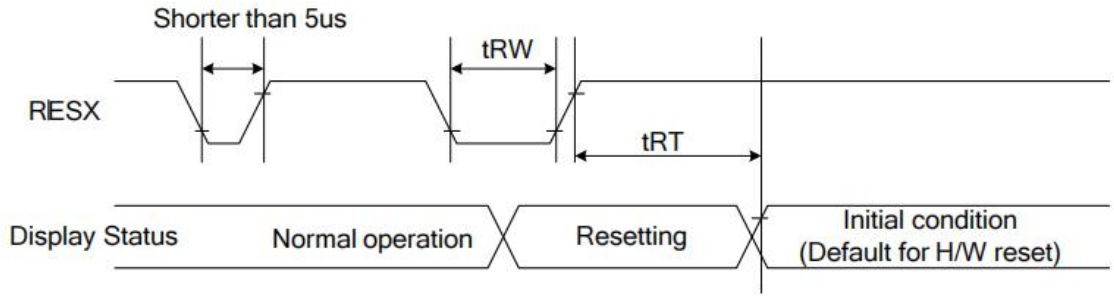

Figure 105: Reset Timing

Table 46: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

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Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 47.*

Table 47: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

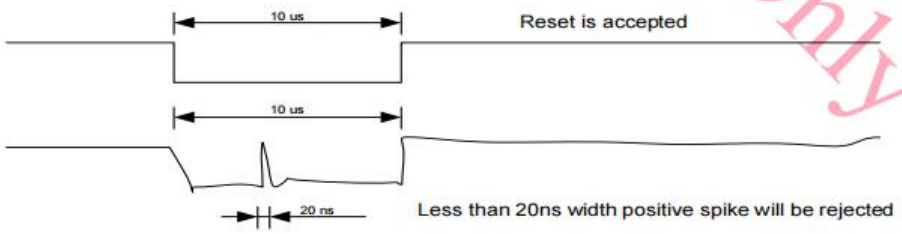

Figure 106: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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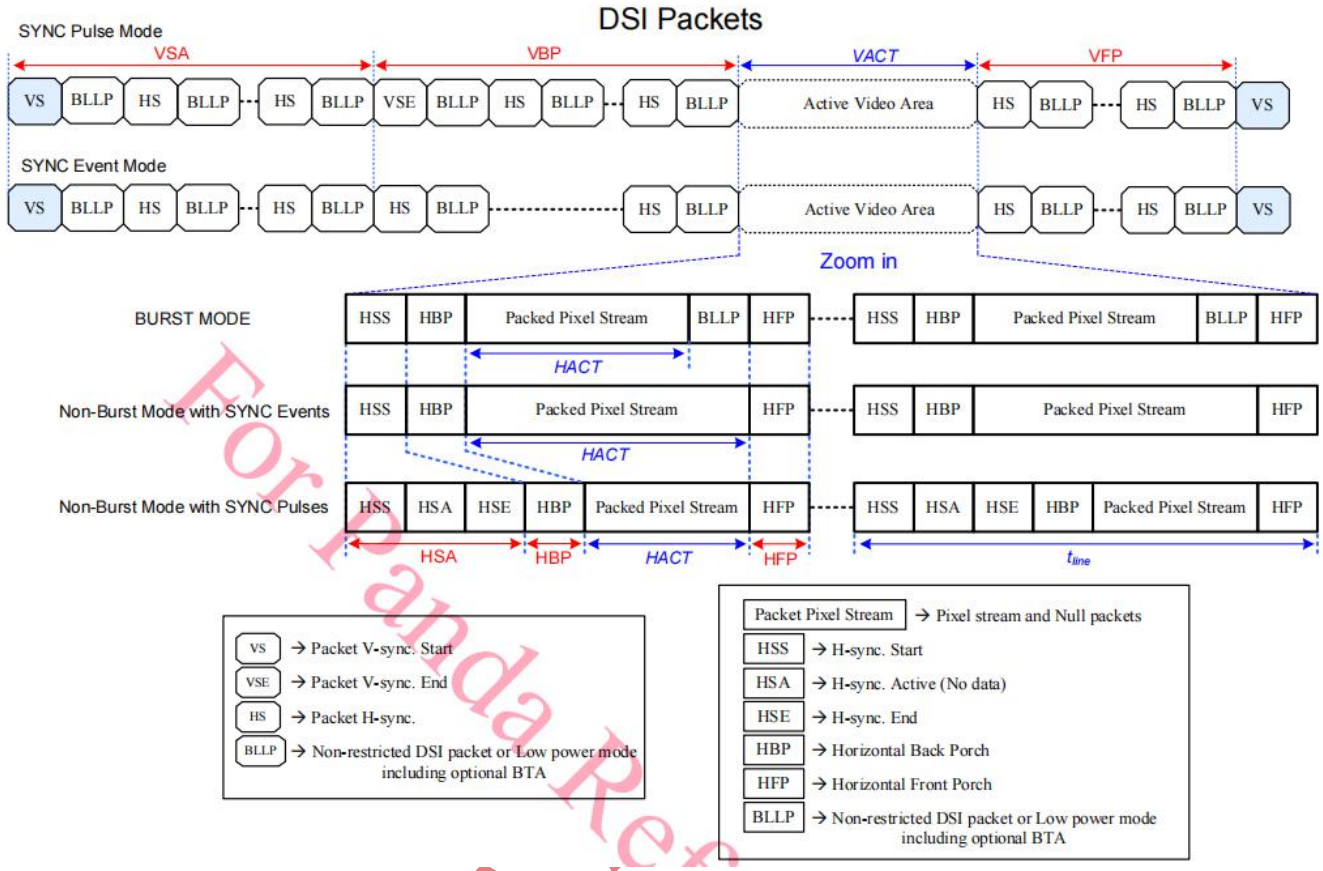
5.5.2 Timing for DSI video mode



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Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR_{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

HSA(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to “Table 38: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

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5.5.3 Timing Parameters

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Vertical low pulse width	VS	-	-	-	-	Line
Vertical front porch	VFP	-	-	-	-	Line
Vertical back porch	VBP	-	-	-	-	Line
Vertical active area	-	VDISP	-	720	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz
HS low pulse width	HS	-	-	-	-	DCK
Horizontal back porch	HBP	-	-	-	-	DCK
Horizontal front porch	HFP	-	-	-	-	DCK
Horizontal active area	HDISP	-	-	1440	-	DCK

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6. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	1000	1200	-	-	Note(4)
NTSC Ratio	S	θ =0°	65	70		%	Note(7)
Luminance	L	θ =0°	450	500	-	cd/m2	Note(5)
Color temperature	Φ	θ =0°	-	8500	-	K	
Luminance uniformity	U_W	θ =0°	80	-	-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	25	35	ms	Note(2)
Color Coordination	W_X	θ =s 0° (Center) Normal viewing angle B/L On	-+0.03	0.3	+0.03	NTSC (x,y)	Note(6)
	W_Y			0.31			
	R_X			0.650			
	R_Y			0.318			
	G_X			0.263			
	G_y			0.565			
	B_X			0.140			
	B_Y			0.086			
Viewing Angle	θ L	C/R>10	-	80	-	Degree	Note(1)
	θ R		-	80	-		
	θ U		-	80	-		
	θ D		-	80	-		

Test Conditions:

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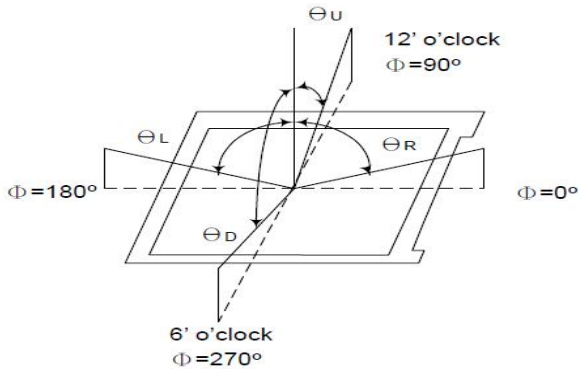
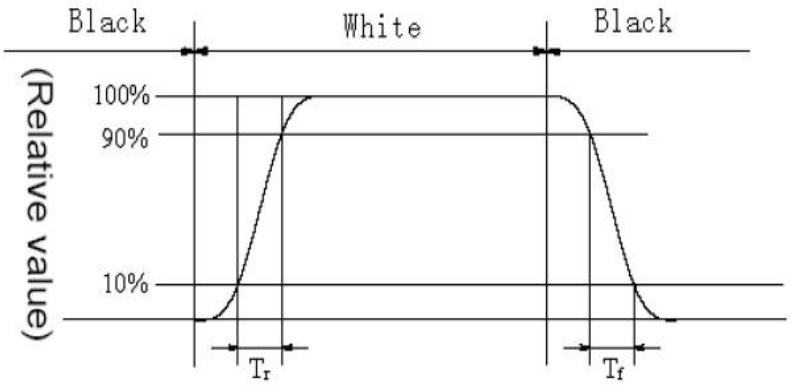
1. the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

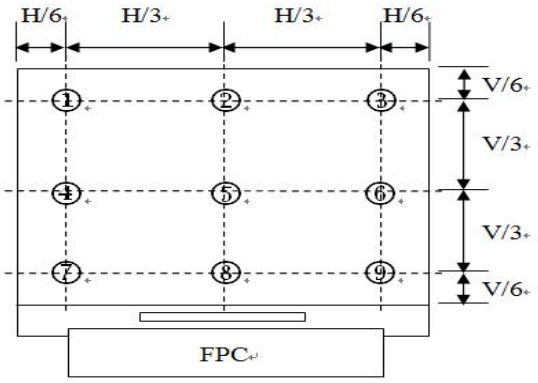


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Min Luminance of white among 9-points}}{\text{Max Luminance of white among 9-points}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

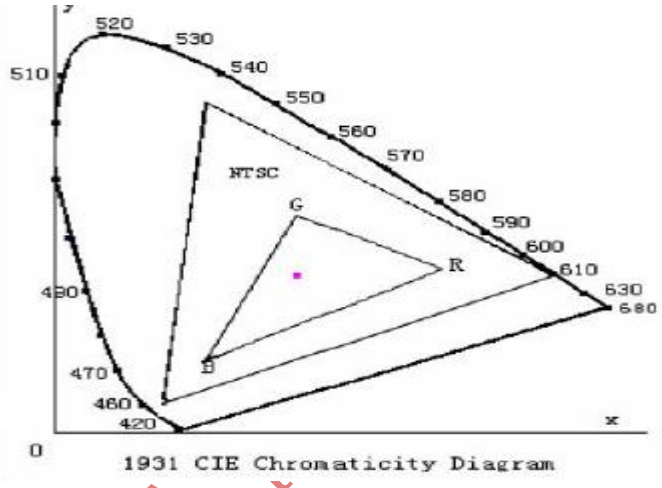
Note 5 Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

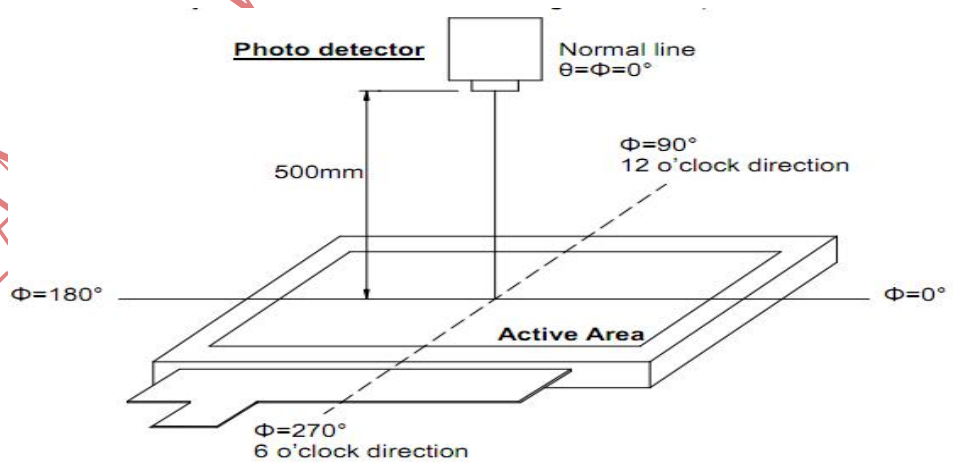
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



7. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min ⇆+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
Package Vibration Test	Frequency: 10Hz~55Hz,Amplitude:1.5mm, 1 hrs for each direction of X, Y, Z	Note2
Packing shock test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	Note2
Flicker test	<18%(-30db) Gamma2.2+/-0.3; Cross talk<=4%	
ESD test	Bare screen: Contact + / - 4KV, air + / - 8Kv; Whole machine: Contact + / - 8Kv, air + / - 12kV	

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

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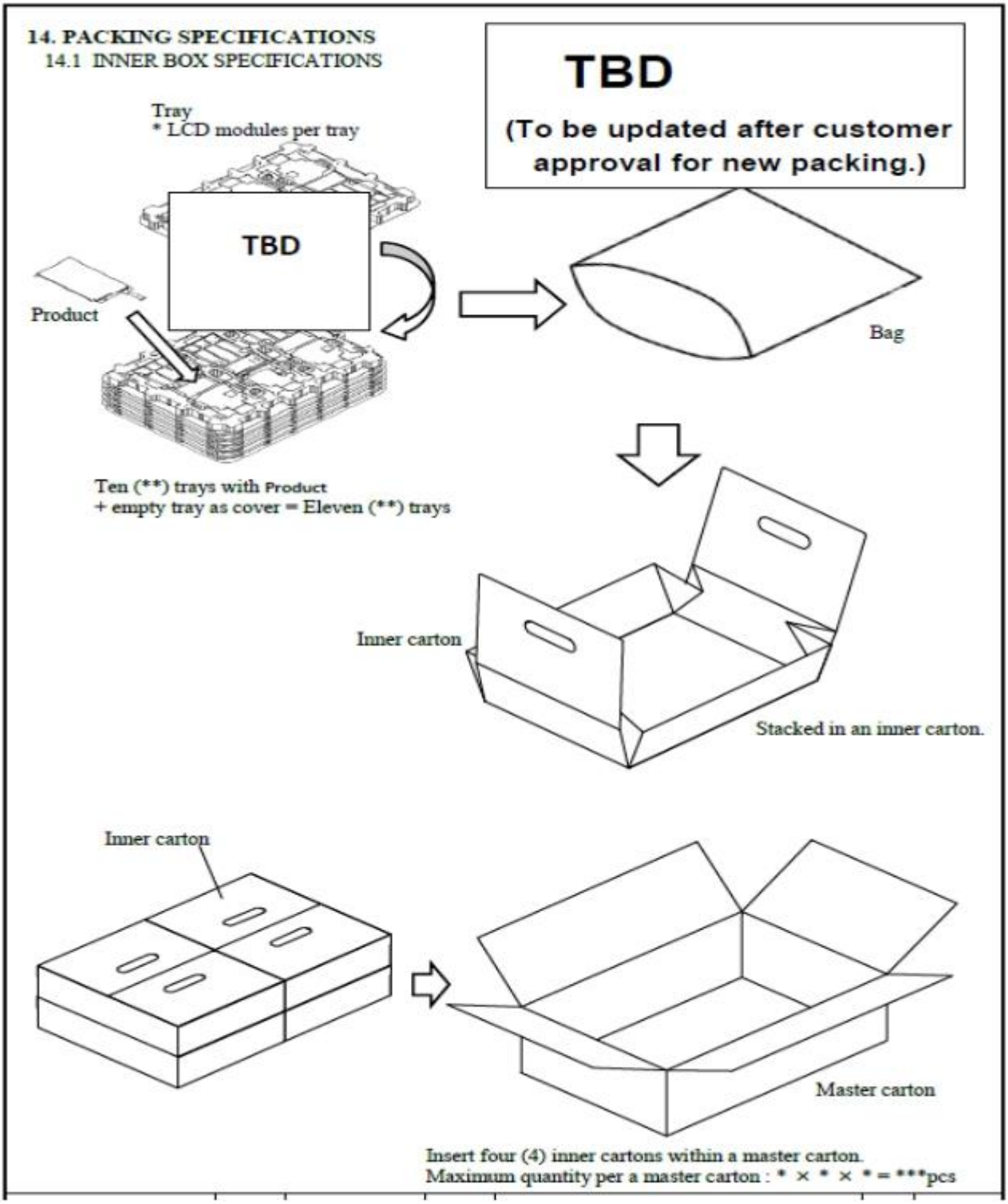
8. PACKAGE DRAWING